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EXTRACTION OF LATERAL DEVICE PARAMETERS AND CHANNEL DOPING PROFILE OF VERTICAL DOUBLE-DIFFUSED MOS TRANSISTORS

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Abstract—An extraction method for device dimensions and the lateral channel doping profile of a vertical double-diffused MOS transistor has been developed. Using C–V characterization and two-dimensional numerical analysis, the lateral device structure parameter could be extracted. The extracted device parameters are in good agreement with the expected values for a fabricated device sample. The proposed method in this paper can be very useful for analysing the electrical characteristics of VDMOS transistors.

1. INTRODUCTION

The conventional VDMOST (vertical double-diffused MOS transistor) is generally fabricated using self-aligned double diffusion process of boron and phosphorus (or arsenic). The double-diffused channel length can be approximated to about 0.8–0.9 times the difference of two vertical diffusion depths. But the diffusions are a two-dimensional process[1] and are not very well defined. The lateral doping profile of the channel cannot be directly measured with any existing profiling techniques. At present, the important device parameters formed laterally in VDMOST, such as channel length and peak doping concentration, are indirectly obtained from conductance measurements[2]. However, the measured parameters by this method reveal some errors because the model is based on strong approximations for the physical behavior of the device. Therefore, a new extraction method with a higher accuracy must be developed.

In order to describe our new methodology, two-dimensional numerical simulation of the capacitance–voltage relationship at a high frequency is performed. Using information from simulation, a new extraction technique for the lateral device structure and the channel doping profile is proposed. The extracted results from the method are compared with the expected value during the device fabrication process.

The VDMOST structure and the simulated results are discussed in Section 2. Section 3 deals with the extraction methodology based on the capacitance–voltage characterizations. The extracted results from a fabricated sample are presented and discussed in Section 4.

2. TWO-DIMENSIONAL NUMERICAL SIMULATION

The numerical simulation to analyse the capacitance–voltage characteristics in VDMOST is performed using ATLAS-II[3]. The cross-sectional view of device is shown in Fig. 1. In the investigated device, the n^+ source length (x_{j-n^+}), channel length (x_{ch}) and drain length (x_d) are 2.1 μm, 4.2 μm and 8.7 μm, respectively. The total gate length (L_T) is the sum of these lengths. The gate oxide thickness (t_{ox}) is 0.1 μm and the doping concentration of n^- epitaxial layer (N_D) generally called the lightly doped drain region, is $3 \times 10^{[illegible]}$ cm^{-3}. The doping concentration of the p region has a two-dimensional Gaussian profile and the peak concentration at the source end is

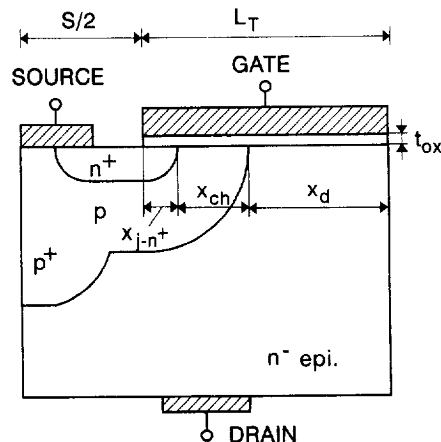

Fig. 1. The cross-sectional view of vertical double-diffused MOS transistor.

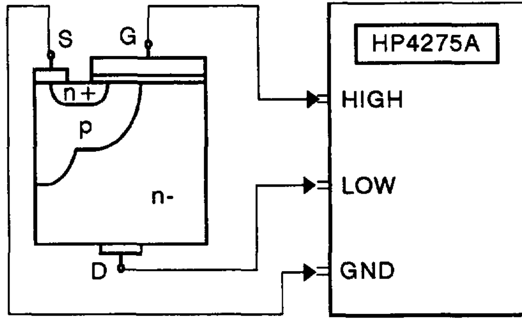

Fig. 2. The electrode configuration for gate–drain capacitance (C_{GD}) measurement.

$2 \times 10^{16}\ cm^{-3}$. The source electrode is contacted to n^+ and p regions simultaneously.

The capacitance between the gate and drain, C_{GD}, is used in the numerical simulation and measurement in order to extract the device parameters. Its electrode connection is shown in Fig. 2. The multi-frequency LCR meter (HP4275A)[4] is used in measurement. A small a.c. voltage of 10 mV at 1 MHz is applied between the high (gate) and low (drain) potential electrodes. Note that the capacitance through the source electrode grounded to d.c. is not included in the measurement because the small a.c. voltage is not applied to the electrode[5].

The simulated capacitance C_{GD} is shown in Fig. 3 and the conceptional charge distributions with the applied d.c. gate biases are shown Fig. 4(a)–(c). When an applied d.c. gate voltage is lower than the threshold voltage of n^- region V_{TD} of about -0.9 V, the n^+ region, p region and n^- region show depletion, accumulation and inversion modes, respectively [see Fig. 4(a)]. In this case, the holes of the strongly inverted n^- region cannot be supplied from the p region because the p region is floated at a.c. Therefore, C_{GD} in this case is the minimum value consisted of metal–oxide–n^- structure capacitance and its value $C_{GD\text{-}MIN}$ is written by:

$$C_{GD\text{-}MIN} = C_{OX} \cdot C_{DM}/(C_{OX} + C_{DM}) \cdot A_{drain}. \quad (1)$$

Here, A_{drain} is the area of n^- region, C_{OX} $(=\epsilon_{ox}/t_{ox})$ is the gate oxide capacitance per unit area and C_{DM} is the depletion capacitance per unit area in n^- region given by:

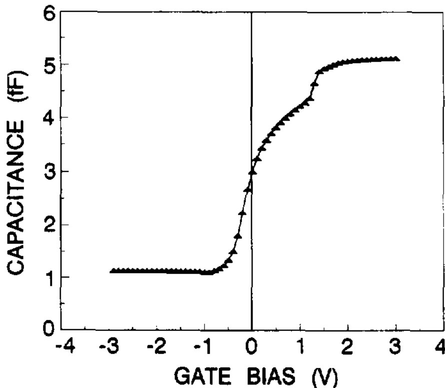

Fig. 3. The simulated gate–drain capacitance curve (C_{GD}).

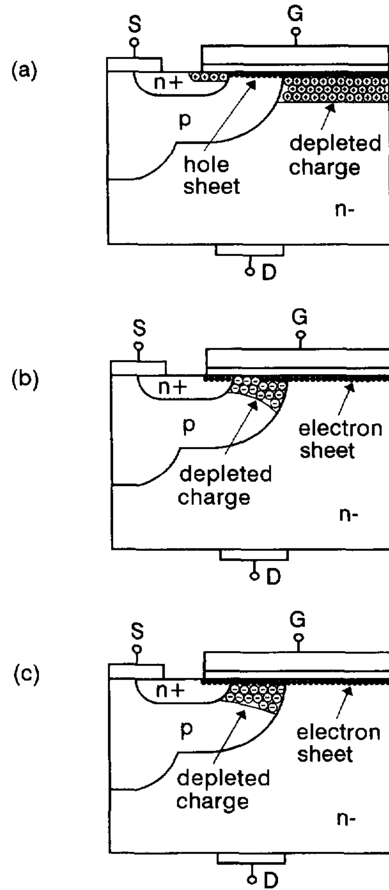

Fig. 4. The conceptional charge distribution in VDMOST with different applied gate d.c. biases: (a) $V_G < V_{TD}$, (b) $V_{TD} < V_G < V_{TE\text{-}MAX}$ and (c) $V_G > V_{TE\text{-}MAX}$.

$$C_{DM} = \frac{\epsilon_{si}}{\sqrt{\frac{2\epsilon_{si}}{qN_D}\psi_D}}, \quad (2)$$

where ψ_D is the surface potential in the strong inverted n^- region. As the gate voltage is larger than V_{TD}, n^- region is changed from strong inversion to depletion and electrons are supplied from n^- region to the partially inverted p region at the drain end as well as to the accumulated n^- region [see Fig. 4(b)]. Then, C_{GD} becomes larger than that of metal–oxide–n^- structure (C_{REF}) as the inverted p region is expanded with gate voltage. The difference of capacitances of C_{GD} and C_{REF} is the oxide capacitance of partially inverted p region. When the gate voltage is larger than $V_{TE\text{-}MAX}$ of about 1.3 V, which is the maximum threshold voltage of channel determined by the peak doping concentration, the electrons in the accumulated n^+ region as well as the p region are supplied from the n^- region [see Fig. 4(c)]. Therefore, C_{GD} undergoes sudden increase at $V_G = V_{TE\text{-}MAX}$ and the capacitance variation at

$V_{TE\text{-}MAX}$, ΔC_{GD}, is the same as the oxide capacitance of n^+ region written by:

$$\Delta C_{GD} = C_{OX} \cdot A_{n+source}, \quad (3)$$

where $A_{n+source}$ is the area of n^+ region. In the case of $V_G > V_{TE\text{-}MAX}$, C_{GD} is the same as the entire gate oxide capacitance and its value, $C_{GD\text{-}T}$, is represented by:

$$C_{GD\text{-}T} = C_{OX} \cdot A_{gate}, \quad (4)$$

where A_{gate} is the total gate area.

The behavior of capacitance–voltage in VDMOST is very different from that of conventional MOST because of the complex device structure. However, the dimensions of device structure can be extracted from the complex behavior of C_{GD} because it responds to the device's lateral dimensions.

3. EXTRACTION METHOD OF DEVICE STRUCTURE AND CHANNEL DOPING PROFILE

3.1. Device structure parameter extraction

The unit cell structure (see Fig. 1) is assumed to be a square type with side length of $2(S/2 + L_T)$, and S and L_T are known parameters. The typical shape of C_{GD} of the unit cell is represented in Fig. 5. In the unit cell of square type, the total gate area A_{gate}, the n^+ source area $A_{n+source}$ and the drain (n^- region) area A_{drain} are represented by:

$$A_{gate} = (2L_T + S)^2 - S^2, \quad (5)$$

$$A_{n+source} = (2L_S + S)^2 - S^2, \quad (6)$$

$$A_{drain} = 4L_D(2L_T + S - L_D), \quad (7)$$

$$L_T = L_S + L_{CH} + L_D, \quad (8)$$

where L_S, L_{CH} and L_D are the n^+ source length, the channel length and the drain length (n^- region), respectively. From eqns (4) and (5), the thickness of the gate oxide is extracted, and L_S and L_D are extracted using eqns (3) and (6), and eqns (1), (2) and (7), respectively. Then, L_{CH} is extracted from the extracted L_S, L_D and eqn (8).

The extracted lengths are different from the metallurgical lengths because L_S is measured from the position with the peak doping concentration in the channel and L_D is calculated without consideration of the overlapped depletion region due to the gate and graded p/n^- junction at the drain end. The comparisons between the metallurgical lengths controlled during the diffusion process and the electrical lengths extracted by the above method are shown in Fig. 6. The difference of n^+ source length, ΔL_1, is estimated to be about 0.2–0.4 μm and it depends on the junction structures of n^+ and p regions. The measured L_D is shorter than the metallurgical length by ΔL_2 because the real depletion region under the gate electrode is a trapezoid structure of depleted charges, $qN_D(L_D + \Delta L_2 - 0.5W_N)W_{GD}$, but it is ideally approximated as a rectangular structure of charges, $qN_D L_D W_{GD}$, in the extraction method. Here, W_N is the depleted width into the n^- region at the graded p/n^- junction and W_{GD} is the depleted width under the gate electrode. As shown in Fig. 7, to keep the same depleted charges between the real

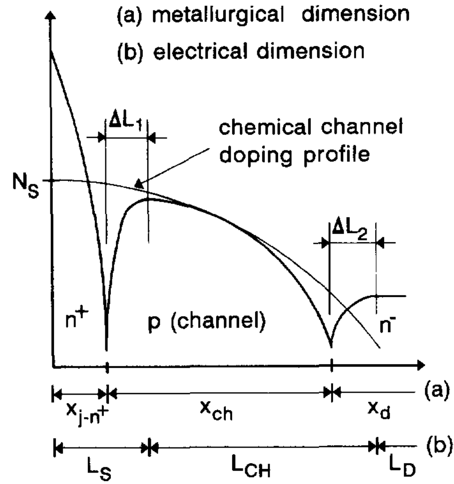

Fig. 6. The comparisons between the metallurgical dimensions and the extracted electrical dimensions.

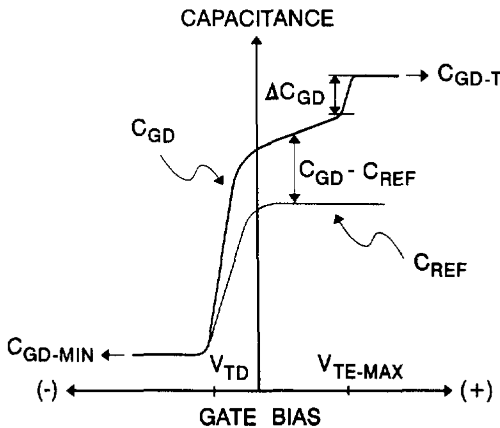

Fig. 5. The typical shape of C_{GD} in VDMOST.

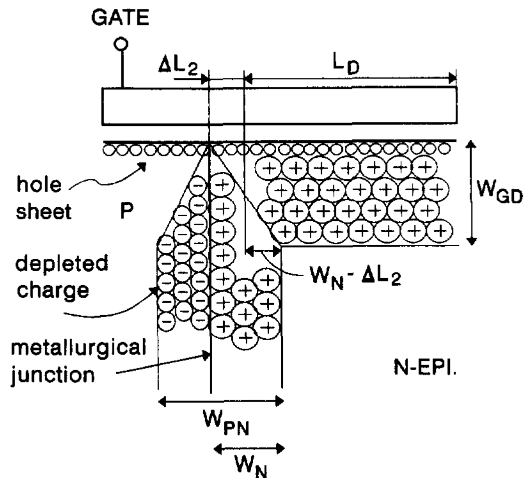

Fig. 7. The schematic view for charge distribution at the graded p/n^- junction to analyse ΔL_2.

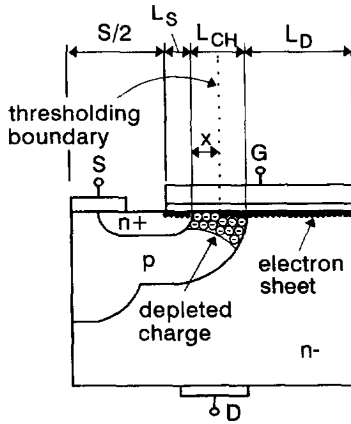

Fig. 8. The charge distribution and thresholding boundary in the case of $V_{TD} < V_G < V_{TE\text{-}MAX}$.

depletion region and approximated depletion region, ΔL_2 should be $0.5W_N$. ΔL_2 is about 0.5–1.0 μm for the junction structure. The relationship between the metallurgical and the extracted lengths are represented as follows:

$$x_{j-n^+} = L_S - \Delta L_1, \quad (9)$$

$$x_{ch} = L_{CH} + \Delta L_1 - \Delta L_2, \quad (10)$$

$$x_d = L_D + \Delta L_2. \quad (11)$$

3.2. Channel doping profile extraction

To derive the doping profile in the channel, the reference capacitance, C_{REF} denoted in Fig. 5, is needed. The capacitance is the metal–oxide–n^- layer structure capacitance with the drain area size. It can be obtained from the theoretical calculation or the measurement of test pattern with an identical MOS capacitor. Figure 8 shows the charge distribution in the junctions for the case of $V_{TD} < V_G < V_{TE\text{-}MAX}$. In Fig. 8, $x = 0$ represents the position at the peak channel doping concentration. The electrons in the partially inverted channel are supplied from the n^- region as mentioned in Section 2. Therefore, the difference between C_{GD} and C_{REF} is equal to the gate oxide capacitance of inverted channel region and is represented by:

$$C_{GD} - C_{REF} = C_{OX} \cdot A_{ch-x}, \quad (12)$$

where the area of partially inverted channel, A_{ch-x}, is derived as:

$$A_{ch-x} = (2L_{CH} + 2L_S + S)^2 - (2x + 2L_S + S)^2. \quad (13)$$

Here, x is the depleted region length in the channel at any given gate bias ($V_{TD} < V_G < V_{TE\text{-}MAX}$) and it can be determined from eqns (12) and (13). The applied gate voltage is the same as the threshold voltage determined by the doping concentration at the thresholding boundary in channel. Therefore, its relationship is written by:

$$V_G = V_{FBX} + \psi_{EX} + \frac{\sqrt{2q\epsilon_{si} N_{CHX} \psi_{EX}}}{C_{OX}}, \quad (14)$$

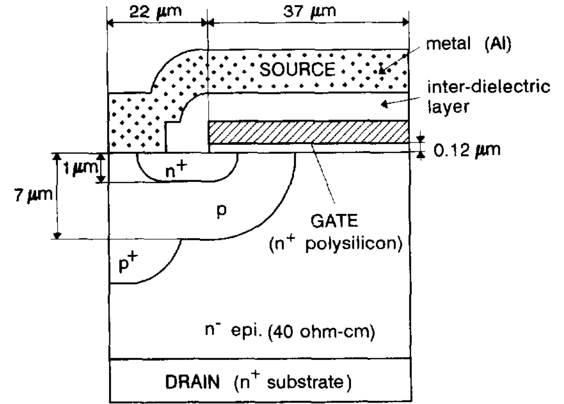

Fig. 9. The schematic cross-section of fabricated VDMOST.

where N_{CHX}, V_{FBX} and ψ_{EX} are the doping concentration, flat-band voltage and surface potential at a position x in the channel, respectively. Using eqns (12)–(14), the channel doping concentration formed laterally can be extracted. Note that the extracted doping concentration shows the net doping profile in electrical channel region (L_{CH} region).

4. FABRICATION, MEASUREMENT AND DISCUSSION

VDMOST used in this work is fabricated using a well-known conventional DMOS process. The schematic cross-section of fabricated sample is shown in Fig. 9. The $S/2$ and L_T in the unit cell are 22 μm and 37 μm, respectively, and the structure of unit cell is of square type with a side length of 118 μm. The device is fabricated on a 40 Ω cm, (100) n type epitaxial layer on n^+ substrate. The p^+ region in the cell is formed, gate oxide of 0.12 μm is grown, polysilicon is deposited and the gate region of VDMOST is defined. Then, the p and n^+ regions in the cell are diffused sequentially from boron and phosphorous implantation sources, respectively. After drive-in to control the junction depths, an inter-oxide layer of 0.8 μm is deposited by CVD, the contact window is opened and the metallization is

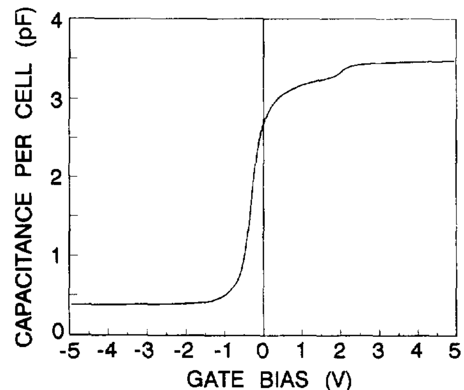

Fig. 10. Measured capacitance–voltage curve per unit cell of fabricated VDMOST.

Table 1. The comparisons of the real lateral dimensions, the extracted electrical dimensions and the re-extracted lateral dimensions

Real lateral dimension	x_{j-n^+}	0.85 μm	0.85 × vertical junction depth
	x_{ch}	5.10 μm	
	x_d	31.05 μm	
Extracted electrical dimension	L_S	1.24 μm	By C–V measurement
	L_{CH}	5.61 μm	
	L_D	30.15 μm	
Re-extracted lateral dimension	x_{j-n^+}	0.94 μm	Using $\Delta L_1 = 0.3\ \mu$m, $\Delta L_2 = 0.75\ \mu$m
	x_{ch}	5.16 μm	
	x_d	30.90 μm	

accomplished. The vertical junction depths of n^+ and p in the cell regions are 1 μm and 7 μm, respectively, confirmed by spreading resistance profile measurement. The p region is doped to 0.5–1.0 kΩ sq^{-1} resistivity, resulting in a threshold voltage of about 2 V.

The measured curve of C_{GD} vs V_G per unit cell of fabricated device is shown in Fig. 10. The applied small a.c. voltage and its frequency are 10 mV and 1 MHz, respectively. The shape of capacitance is the same as the numerically simulated result discussed in Section 2. $C_{GD\text{-}T}$, ΔC_{GD} and $C_{GD\text{-}MIN}$ in the unit cell are 3.4508, 0.0647 and 0.3797 pF, respectively. From $C_{GD\text{-}T}$, and eqns (4) and (5), the gate oxide thickness of 1199.59 Å is extracted and it is in excellent agreement with the expected oxide thickness from the process. The device parameter lengths extracted from ΔC_{GD}, $C_{GD\text{-}MIN}$ using the method proposed in Section 3, are listed in Table 1. The lateral dimensions expected from the diffusion process with the two-dimensional effect and the re-extracted lateral dimensions, corrected by eqns (9)–(11) using typical $\Delta L_1 = 0.3\ \mu$m and $\Delta L_2 = 0.75\ \mu$m, are listed together. The re-extracted device dimensions are within a small error range of about 1–11% from the expected values.

In Fig. 11, the extracted lateral doping profile in the channel using eqns (12)–(14) is represented. In this figure, x is the channel distance from the position with peak doping concentration. For the extraction, C_{REF} is calculated theoretically in this work. The peak doping concentration is about 2×10^{16} cm^{-3}, which agrees very well with $V_{TE\text{-}MAX}$ of about 2 V. The doping concentrations in the region above 3 μm cannot be extracted exactly because the difference between C_{GD} and C_{REF} is very small and the variation of capacitance with the gate voltage becomes very large at $V_G < 0$. However, the extracted doping concentration profile represented in Fig. 11 is sufficient to estimate the entire doping profile. The lateral doping profile of the channel shown in Fig. 6 can be given by:

$$N_{CHX} = N_S \operatorname{erfc}\left(\frac{x + L_S}{x_P}\right) \tag{15}$$

where N_S is the surface doping concentration at gate edge and x_P is the characteristic length of diffusion. From the extracted doping concentration, N_S and x_P are found to be 6×10^{16} cm^{-3} and 3 μm, respectively. For comparison, the doping profile calculated from eqn (15) is represented in Fig. 11, too.

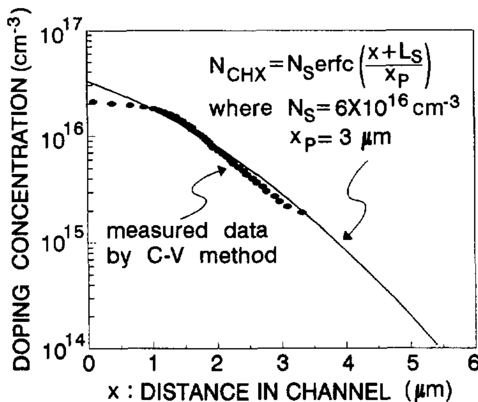

Fig. 11. The extracted lateral channel doping concentration from fabricated VDMOST.

Considering the tolerances of process and electrical characterization, the extracted dimensions and doping profile in the channel are in good agreement with those of fabricated VDMOST. Therefore, the proposed extraction method of the device structure and the lateral doping profile in this work is acceptable for analysing and optimizing VDMOST. Also, it is expected that this method can be extended for analyzing double-diffused channel devices, such as LDMOST (lateral DMOST), IGBT (insulated gate bipolar transistor), LIGBT (lateral IGBT) and MCT (MOS controlled thyristor), if test patterns are made properly to measure the capacitance–voltage relationship of the device.

5. CONCLUSION

An extraction method of the device structure and the channel doping profile formed laterally in VDMOST is proposed in this paper. To set up the methodology, the gate–drain capacitance characteristics in VDMOST are analysed through two-dimensional numerical simulation. Using this information, the device parameter extraction method could be formulated from the variation of capacitance between gate and drain. The extracted device structure, and lateral channel doping profile using the method are in a good agreement with the controlled value in process. The proposed extraction methodology will be valuable for analysing and

optimizing the various power devices with double-diffused channel structure as well as VDMOST.

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