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LETTER

GEOMETRICAL PARAMETERS AND LATERAL CHANNEL DOPING PROFILE EXTRACTION IN A VERTICAL IGBT BY *C–V* MEASUREMENTS

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Abstract—An extraction method for device dimensions and lateral channel doping profiles of a VIGBT (vertical insulated-gate bipolar transistor) has been developed. Through two-dimensional numerical analysis and *C–V* characterizations, the lateral device structure parameters could be extracted. The extracted device parameters are in a good agreement with the expected values of fabricated devices. The method proposed in this paper can be very useful for analyzing the electrical characteristics of a VIGBT. © 1998 Published by Elsevier Science Ltd. All rights reserved

1. INTRODUCTION

In a VIGBT (vertical insulated-gate bipolar transistor), used widely for high voltage applications, it is very important to extract the lateral device structure parameters such as the channel length and the doping profile in order to understand and design the electrical performances. Nevertheless the extraction of structural parameters is not easy because the channels in the VIGBT are formed by the self-aligned double diffusion process of boron and phosphorus (or arsenic). So, a reasonable extraction method with a higher accuracy must be developed. Fortunately, in the case of a VDMOST (vertical double-diffused MOS transistor) with a similar device structure except for the substrate type, the useful extraction method based on capacitance–voltage characterization has been studied[1].

In order to confirm our new methodology to extract the device structure parameters of the VIGBT, two-dimensional numerical simulations of the *C–V* relationship at a high frequency for the VIGBT are performed. Then, using the analyzed information, the lateral device structure and channel doping profile are extracted from the fabricated sample and compared with the controlled values during the device fabrication process.

2. NUMERICAL SIMULATION FOR THE *C–V* RELATIONSHIP AND EXTRACTION METHOD OF LATERAL DEVICE PARAMETERS IN A VIGBT

2.1. *Two-dimensional numerical simulation*

The cross-sectional view of device and the geometrical parameters to be used in the numerical simulation, which is performed using ATLAS-II[2], are shown in Fig. 1. These are the same as those in the previous report[1] except for a p^+ substrate of 1×10^{20} cm^{-3}.

The simulated capacitance between gate and anode, C_{GA}, of the VIGBT is shown in Fig. 2 with the gate-to-drain capacitance, C_{GD}, of the VDMOST with n^+ instead of p^+ substrate to compare the behaviors. With the real measurement, the anode and the drain electrodes are grounded to dc. A VIGBT can be considered as a VDMOST in series with a n^-/p^+ diode at the anode. Therefore, C_{GA} is affected by the diode junction capacitance, C_J, and so it will be very different from the C_{GD} of a VDMOST. So, this capacitance can be represented by

$$C_{GA}=\frac{C_{G-n^-}C_J}{C_{G-n^-}+C_J}. \quad (1)$$

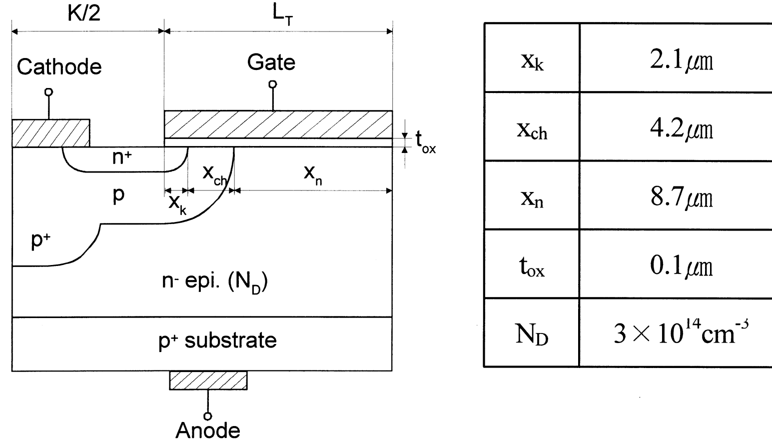
Here, C_J can be calculated as n^-/p^+ diode capacitance at the external zero bias because there is no interaction between the surface depletion region below the gate electrode and the bulk depletion region at the anode junction in the thick n^- epitaxial layer. Therefore, the gate-to-n^- capacitance C_{G-n^-}, which is the same as C_{GA} in the case of VDMOST, can be calculated easily by

$$C_{GD-VIGBT}=C_{G-n^-}=\frac{C_JC_{GA}}{C_J-C_{GA}}. \quad (2)$$

The $C_{GD\text{-}VIGBT}$ calculated from Equation (2) using $C_J=1.55$ fF simulated at the zero bias is shown in Fig. 2, too, and it can be found that $C_{GD\text{-}VIGBT}$ is identical to the C_{GD} of VDMOST. Therefore, the lateral structure parameters and the channel doping profile of VIGBT can be also extracted by the verified method for a VDMOST[1] using the converted $C_{GD\text{-}VIGBT}$ from C_{GA}.

2.2. *Extraction of the lateral dimensions and the channel doping profile*

For $C_{GD\text{-}VIGBT}$ with gate bias V_G, the necessary capacitances to be used in the extraction of the elec-



x_k	2.1 μm
x_{ch}	4.2 μm
x_n	8.7 μm
t_{ox}	0.1 μm
N_D	3×10^{14} cm^{-3}

Fig. 1. The cross-sectional view of the vertical insulated-gate bipolar transistor used in the simulation and the geometrical parameters.

trical and metallurgical device dimensions are (1) C_{MIN} at the high negative gate bias, (2) ΔC jumped around the threshold voltage of device and (3) C_T at the high positive gate bias. C_{MIN} means the minimum capacitance of the gate electrode–oxide–n$^-$ structure when the applied gate voltage is lower than the threshold voltage of the n$^-$ region V_{TD} of about –0.9 V in this investigated device. So, this capacitance value is determined by the n$^-$ area beneath the gate oxide and it can be represented by

$$C_{MIN} = \frac{C_{OX}C_{DM}}{C_{OX}+C_{DM}} \times [4L_N(2L_T+K-L_N)], \quad (3)$$

where C_{OX} and C_{DM} are the gate oxide capacitance and the depletion capacitance per unit area in the n$^-$ region, and $4L_N(2L_T+K-L_N)$ is the n$^-$ area in the unit cell assumed to be a square type with a side length of $2(K/2+L_T)$. Here K and L_T are the cathode and the gate electrode widths on the layout, respectively, and L_N is the electrical n$^-$ length. ΔC increased rapidly around the maximum threshold voltage $V_{TE\text{-}MAX}$ in the double-diffused channel, about 1.5 V in this device, and is formed by the connection of the accumulated electron sheets in the n$^-$ and n$^+$ cathode regions. Therefore ΔC is equal to the gate oxide capacitance of the n$^+$ cathode region and can be written by

$$\Delta C = C_{OX} \times [(2L_K+K)^2 - K^2], \quad (4)$$

where L_K is the electrical cathode overlap length. When the gate voltage is larger than $V_{TE\text{-}MAX}$, the capacitance is saturated to C_T which is the same as the entire gate oxide capacitance and is represented by

$$C_T = C_{OX} \times [(2L_T+K)^2 - K^2]$$
$$= C_{OX} \times \{[2(L_K+L_{CH}+L_N)+K]^2 - K^2\}, \quad (5)$$

where L_{CH} is the electrical double-diffused channel length. Therefore, the electrical lateral dimensions of L_K, L_{CH} and L_N can be found using Equations (3)–(5) and the gate oxide thickness can be also calculated from Equation (5). When it is considered in extracting that the difference between the electrical and the metallurgical dimensions is due to the impurity compensation and the charge sharing effects, the exact metallurgical dimensions can be also extracted at the same time. The formulas for the metallurgical lateral dimensions are well established in the previous report[1] as

$$x_k = L_K - \Delta L_1, \quad (6)$$

$$x_{ch} = L_{CH} + \Delta L_1 - \Delta L_2, \quad (7)$$

$$x_n = L_N + \Delta L_2, \quad (8)$$

where ΔL_1 is the difference of the n$^+$ cathode and ΔL_2 is the difference of the n^- region.

In order to extract the lateral doping profile of the double-diffused channel, the reference capacitance for a two-terminal gate electrode–oxide–n$^-$ MOS capacitor, C_{REF}, should be calculated theoretically or measured through the proper test pattern. In the $C_{GD\text{-}VIGBT}$ curve, when the gate voltage is applied between V_{TD} and $V_{TE\text{-}MAX}$, the capacitance includes the gate oxide capacitance of the partially inverted channel as well as the gate electrode–oxide–n$^-$ MOS capacitance. So, the capacitance behavior in this bias region can be described by

$$C_{GD-VIGBT} = C_{REF} + C_{OX} \times [(2L_{CH}+2L_K+K)^2 - (2x+2L_K+K)^2], \quad (9)$$

where the second term is the gate capacitance of partially inverted channel and x is the depleted region, which means the non-inverted region at the heavily doped p-type channel at any given gate bias ($V_{TD} < V_G < V_{TE\text{-}MAX}$). The applied gate voltage is

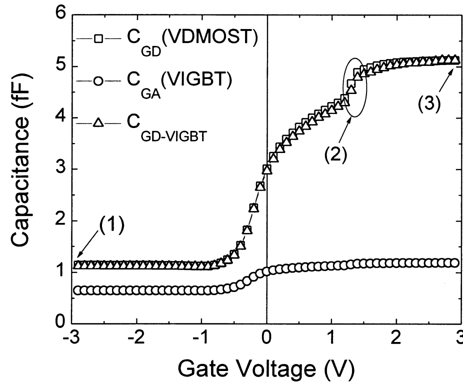


Fig. 2. The simulated results of C_{GA} in the VIGBT, C_{GD} in the VDMOST and $C_{GD\text{-}VIGBT}$ re-calculated using $C_J = 1.55$ fF. In this figure, (1), (2) and (3) are C_{MIN}, ΔC and C_T, respectively.

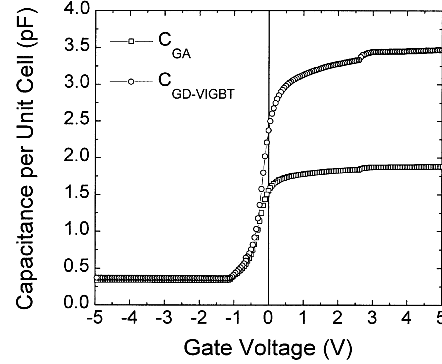


Fig. 4. (a) Measured C_{GA} and (b) re-calculated $C_{GD\text{-}VIGBT}$ by $C_J = 4.096$ pF per unit cell of a fabricated VIGBT.

the same as the local threshold voltage determined by the doping concentration at the thresholding boundary x in channel. Therefore, the net channel doping concentration laterally can be extracted through the extracted position x and the applied gate voltage at that time using Equation (9).

3. FABRICATION, MEASUREMENT AND DISCUSSION

The VIGBT used in this work is fabricated using a well-known conventional DMOS process. The schematic cross section of fabricated sample is shown in Fig. 3. The $K/2$ and L_T are 22 and 37 μm, respectively, and the unit cell structure is of square type with a side length of 118 μm. The device is fabricated on a 50 Ω cm, (100) n-type epitaxial layer on a p^+ substrate. The n-buffer layer of 0.115 Ω cm is formed between the n-type epitaxial layer and the p^+ substrate to prevent the cathode-to-anode punchthrough. The p^+ region in the cell is formed, a gate oxide of 1200 Å is grown, n-type polysilicon is deposited and the gate region of the VIGBT is defined. Then the p and n^+ regions in the cell are diffused sequentially from boron and phosphorous implantation sources, respectively. After drive-in to control the junction depths, the inter-oxide layer of 0.8 μm is deposited by CVD, the contact window is opened and the metallization is accomplished. In this device, the vertical junction depths of the n^+ and p regions in the cell are 1 and 4 μm, respectively, confirmed by spreading resistance profile measurements. The p region is adjusted to have a threshold voltage ($V_{TE\text{-}MAX}$) of about 3 V.

The measured curve of C_{GA} versus V_G per unit cell of fabricated device is shown in Fig. 4. The multi-frequency LCR meter (HP4275A)[3] is used in the measurement. The applied small AC voltage and its frequency are 10 mV and 1 MHz, respectively. Using a serial connection mode of resistor and capacitor, C_J is also measured through the cathode and anode electrodes under the high gate DC bias of 10 V for connecting the n^+ cathode to the n^- region through the smallest channel resistance. The measured C_J is 4.096 pF per unit cell and it is also comparable to that of a simple $n^+/n^-/n$-

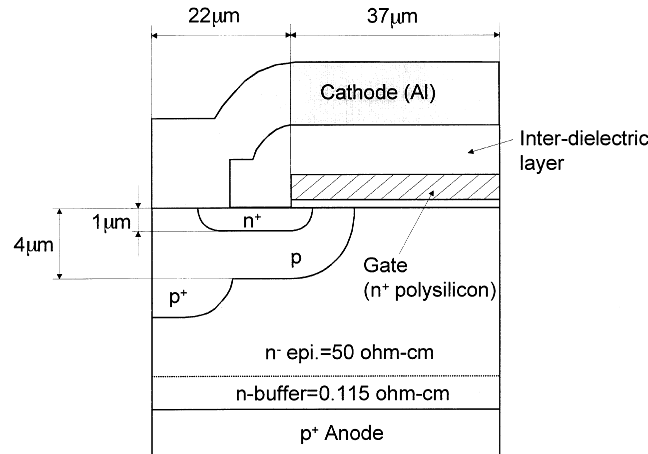


Fig. 3. The schematic cross section of a fabricated VIGBT.

Table 1. The comparison of the real lateral dimensions, the extracted electrical and the metallurgical dimensions

Parameters	Values (μm)	Remarks
	Real lateral dimensions	
X_k	0.85	$0.85 \times$ vertical junction depth
X_{ch}	2.55	
X_n	33.60	
	Extracted electrical dimensions	
L_K	1.21	by C–V measurement
L_{CH}	2.89	
L_N	32.90	
	Re-calculated metallurgical dimensions	
X_k	0.91	using $\Delta L_1 = 0.3$ μm and $\Delta L_2 = 0.75$ μm
X_{ch}	2.44	
X_n	33.65	

buffer/p$^+$ diode within an 8% error range. The re-calculated $C_{GD\text{-}VIGBT}$ per unit cell using C_J and Equation (2) is also shown in Fig. 4. From $C_{GD\text{-}VIGBT}$ in this plot, C_T, ΔC and C_{MIN} in the unit cell are 3.4691 pF, 0.0636 pF and 0.3677 pF, respectively. The extracted gate oxide thickness is 1193.27 Å in excellent agreement with the process data. The extracted electrical lateral dimensions from C_T, ΔC and C_{MIN} using the proposed method are listed in Table 1. The metallurgical dimensions re-calculated using the typical $\Delta L_1 = 0.3$ μm and $\Delta L_2 = 0.75$ μm are also listed together, and these values are within a small error range below 7% from the expected values calculated under the general assumption of lateral depth = $0.85 \times$ vertical depth.

In Fig. 5, the extracted lateral channel doping profile using the theoretical C_{REF} is represented. In this figure, x is the channel distance from the position with peak doping concentration. The extracted peak concentration is about 2.7×10^{16} cm^{-3} and it agrees very well with the threshold voltage of 3 V of the fabricated device. The doping concentration in the region of $x > 2.8$ μm cannot be extracted properly because the difference between $C_{GD\text{-}VIGBT}$ and C_{REF} is very small and the variation of capacitance with the gate bias becomes very large at $V_G < 0$ V. However, the entire doping profile can be sufficiently estimated from the extracted doping concentration represented in Fig. 5. The theoretical lateral doping profile of

$$N_{CHX} = N_S \operatorname{erfc}\left(\frac{x + L_K}{x_P}\right) \quad (10)$$

is also plotted in Fig. 5 to compare with the extracted doping concentration. The surface boron (p-type) concentration at the gate edge N_S are found to be 7.5×10^{16} cm^{-3} and the characteristic length of diffusion x_P is 2.6 μm.

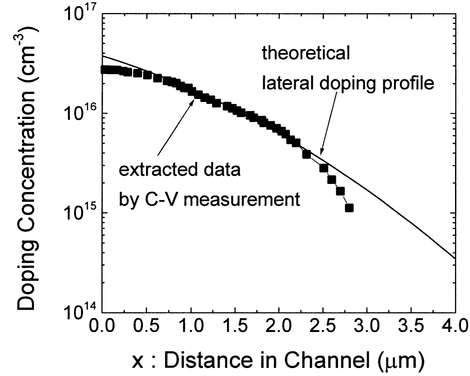


Fig. 5. The extracted lateral channel doping concentration from the fabricated VIGBT and the theoretical doping profile.

4. CONCLUSION

In this paper, an extraction method of the lateral device dimensions and the channel doping profile formed laterally in a VIGBT is proposed. To set-up the methodology, the capacitance behavior is analyzed through the numerical simulation in prior to measurement. This is basically based on the method confirmed in VDMOST. In order to analyze like VDMOST, the gate-to-anode capacitance (C_{GA}) should be converted to the gate-to-n$^-$ capacitance ($C_{GD\text{-}VIGBT}$) using the anode junction capacitance (C_J). The extracted device dimensions and the lateral channel doping profile are in a good agreement with the reasonable error range. Therefore the proposed extraction methodology for VIGBT will be valuable for analyzing and optimizing the various power device based on the double-diffused channel structure

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