

# Baseband stage for WCDMA direct conversion receiver with high dynamic range and accurate temperature compensation

Seonghan Ryu, Sangsu Jin, Seunghyun Lee, Huijung Kim, Jongryul Lee and Bumman Kim

A highly integrated baseband stage, which adopts a new configuration for the wideband code-division multiple access (WCDMA) direct conversion receiver (DCR), is described. The baseband stage satisfies all requirements of the WCDMA DCR and consists of opamp-RC channel select filters and variable gain amplifiers with linear-in-dB gain control. It achieves a high dynamic range of 85 dB with  $\pm 1.5$  dB accuracy over a temperature variation from  $-25$  to  $85^\circ\text{C}$ ,  $16.5$  nV/ $\sqrt{\text{Hz}}$  input-referred noise,  $+20$  dBV out-of-band IIP3 and  $+70$  dBV out of band IIP2. The baseband stage is fabricated using a  $0.35$   $\mu\text{m}$  SiGe BiCMOS process and consumes a total current of  $11$  mA/CH from a  $2.7$  V supply.

**Introduction:** The direct conversion architecture is obviously favoured since it can eliminate intermediate frequency (IF) circuitry. In WCDMA DCR, after downconversion to zero-IF, the baseband chain performs two major roles: channel selection and gain adjustment for accommodating a  $100$  dB dynamic range input signal. The environment that the chain faces is crucial since strong out-of-band interferers are downconverted together with weak in-band signals by the zero-IF mixer. These interferers produce intermodulation products falling in-band after channel selection, which degrade the bit error rate (BER) of the receiver. Thus, the chain should have high IIP3 and IIP2 for high interferers and low noise figure (NF) for weak in-band signals. It is hard to realise the high linearity, low NF and low power consumption simultaneously since they are in trade-off. DC offsets are also problematic in DCR. Offset arises from inherent device mismatches and leakage of the LO signal into the LNA and mixer inputs. And it degrades IIP2 and the I-Q path balance of the chain and may bring the receiver into saturation due to high baseband gain.

This Letter describes a new circuit configuration for each block of the baseband chain to optimise the performance for linearity, NF and power consumption. The circuit schemes for the DC-offset cancellation and accurate decibel-linear gain control with temperature compensation are also presented.

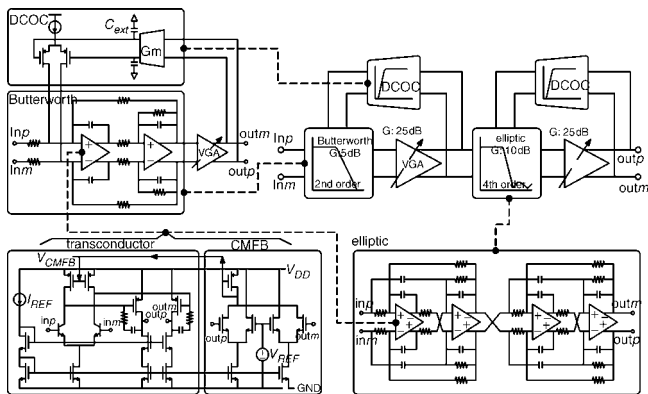


Fig. 1 Simplified diagram of proposed baseband stage

**Proposed configuration of baseband chain:** A filter with elliptic response is favoured for channel selection owing to the steep frequency magnitude response, and the opamp-RC filter is preferred over the transconductance-C (Gm-C) filter with insufficient linearity. The sixth-order elliptic filter based on the opamp-RC can achieve about  $60$  dB out-of-band attenuation. However, if the three biquad blocks are simply combined in cascade, there remains a problem about trade-off among linearity, power consumption and NF. The filter needs high power consumption to maintain high linearity, which worsens NF. If the filter gain is raised to improve NF, linearity is degraded. Fig. 1 shows a simplified diagram of the proposed baseband stage, which adopts partitioning of the chain between gain and filtering for an optimum solution.

The sixth-order elliptic filter is divided into two stages: second-order and fourth-order filters, and the second-order filter is replaced by a Butterworth filter, which has better ripple characteristics. The VGA comprises two stages and each stage, which has a gain of about  $25$  dB, is placed between the two filters and at the end of the chain to relax the filter NF requirement. The filters also have gains of  $5$  and  $10$  dB to keep a low NF. In this way, the optimum solution for high baseband gain of about  $65$  dB, low NF, and low power consumption is achieved. Simultaneously, the linearity specification for WCDMA DCR is also satisfied without any particular linearisation technique. A DC offset canceller (DCOC) is also shown in Fig. 1. The offset of each VGA output is detected by the Gm cell, and it is cancelled at the filter input via feedback loop with external capacitors. The Gm cell and capacitors are tuned for a cutoff frequency of about  $2$  kHz, which does not significantly degrade the BER of the DCR.

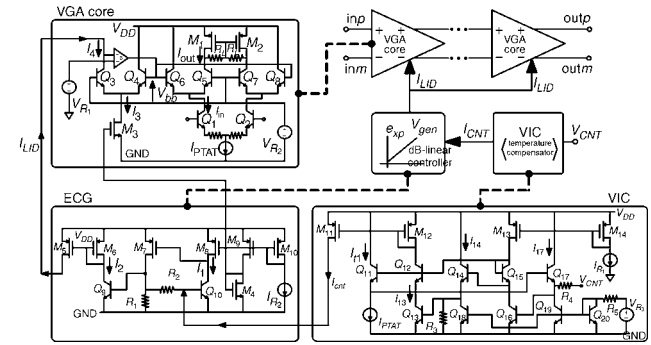


Fig. 2 Simplified schematic diagram of VGA

**Implementation of VGA:** The gain control circuit blocks and simplified schematic diagram of the VGA are shown in Fig. 2. The VGA comprises a voltage-to-current converter (VIC) for temperature compensation, an exponential current generator (ECG) for dB-linear gain control and VGA core gain stages. The core adopts a variable-gain quad based on signal summation for low distortion and low noise [1, 2]. If the differential pairs  $Q_5$ - $Q_6$  and  $Q_7$ - $Q_8$  do not exist, the overall gain of the VGA core is simply  $g_m R_L$ , but the differential pairs control the current flow through the load  $R_L$ . Thus, the actual gain is multiplied by the current gain variation factor  $G_f$ . For dB-linear gain variation, the VGA adopts ECG which uses exponential characteristics of bipolar transistors [3]. The gain control current  $I_{CNT}$  is applied to the base of  $Q_{10}$  and generates a voltage of  $I_{CNT} R_2$ , which reduces  $I_2$ , in comparison with  $I_1$ , in an exponential manner. Current mirrors comprising  $M_3$ - $M_6$  are adjusted so that  $I_2/I_1 = I_4/I_3$ , and differential pairs  $Q_3$ - $Q_8$  have the same base-to-base voltage  $V_{bb}$  for  $I_{out}/I_{in} = I_4/I_3$ . As a result, the gain variation is

$$G_f = \frac{I_{out}}{I_{in}} = \frac{I_4}{I_3} = \frac{I_2}{I_1} = \exp\left(\frac{-I_{CNT} R_2}{V_T}\right) \quad (1)$$

In (1), temperature compensation is required because  $V_T (=KT/q)$  linearly depends on temperature  $T$ . In the VIC of Fig. 1, if we assume all the transistors and resistors are identical, the sum of the base-emitter voltages of  $Q_{13}$ ,  $Q_{14}$  and  $Q_{15}$  is equal to that of  $Q_{16}$ ,  $Q_{17}$  and  $Q_{11}$ . As the base-emitter voltages of  $Q_{15}$  and  $Q_{16}$  are equal, the sum of the base-emitter voltages of  $Q_{13}$  and  $Q_{14}$  is equal to that of  $Q_{17}$  and  $Q_{11}$ . Thus, the product of the currents  $I_{13}$ ,  $I_{14}$  is equal to that of the currents  $I_{17}$ ,  $I_{11}$ . Currents  $I_{14}$ ,  $I_{17}$  and  $I_{CNT}$  are given by

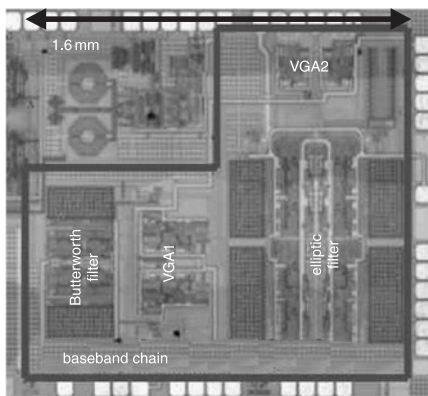
$$I_{14} = \frac{V_{R_3} - V_{BE}}{R} + \frac{V_{BE}}{R} = \frac{V_{R_3}}{R}, \quad (2)$$

$$I_{17} = \frac{V_{R_3} - V_{BE}}{R} - \frac{V_{CNT} - V_{BE}}{R} = \frac{V_{R_3} - V_{CNT}}{R}$$

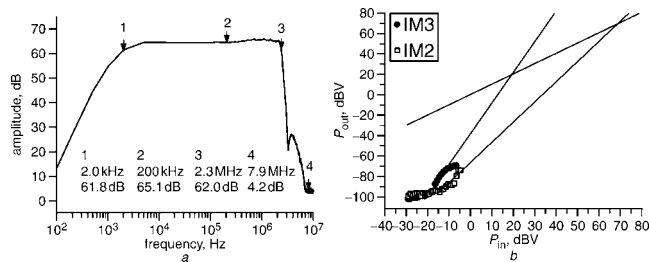
$$I_{CNT} = I_{13} = I_{11} \frac{I_{17}}{I_{14}} = I_{11} \left(1 - \frac{V_{CNT}}{V_{R_3}}\right) \quad (3)$$

From (2) and (3),  $I_{CNT}$  is linearly controlled by  $V_{CNT}$  and is a PTAT current due to PTAT current  $I_{11}$  [4]. This temperature compensation technique is adopted in our VGA. In (1), the voltage drop formed by  $I_{CNT}$  through  $R_2$  is also a PTAT, and its temperature dependence is cancelled with  $V_T$ . Thus, temperature stabilisation of the VGA is achieved.

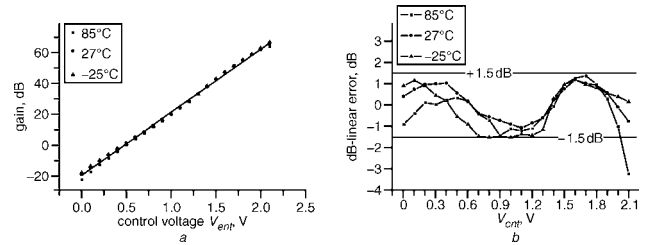
**Measurements:** Fig. 3 shows a microphotograph of the chip. The measured frequency response of the filter is shown in Fig. 4a. The 3 dB band of the chain is 2.3 MHz. The corner frequency of the DCOC is about 2 kHz, the out-of-band attenuation is above 60 dB and the DC offset at the chain output is lower than 10 mV at maximum gain with input offset of about 50 mV. The out-of-band IIP2 and IIP3 are measured with 10, 10.2 MHz and 10, 20.2 MHz test signals, respectively. As shown in Fig. 4b, the measured IIP2 and IIP3 of the chain are 70 and 20 dBV, respectively, and the measured input referred noise is 16.5 nV/ $\sqrt{\text{Hz}}$ . Fig. 5 shows gain of the chain and dB-linear error against control voltage  $V_{ctrl}$  at 1 MHz. A linear-in-dB gain control over a dynamic range of about 85 dB (from -20 to 65 dB) is achieved via the proposed control circuit, and the gain error within  $\pm 1.5$  dB over temperature variation from -25 to 85°C is also achieved.



**Fig. 3** Microphotograph of baseband stage with  $1.6 \times 1.1$  mm chip area



**Fig. 4** Frequency response and graphical extrapolation  
 a Frequency response of the baseband stage  
 b Graphical extrapolation of IIP2 and IIP3



**Fig. 5** Gain and dB-linear error  
 a Gain of the baseband stage  
 b dB-linear error against control voltage

**Conclusion:** A highly integrated baseband stage is proposed. The fabricated baseband stage features a high dynamic range of 85 dB with maximum gain of 65 dB, low noise figure and low power consumption. Simultaneously, the linearity specification for the chain is also satisfied by properly partitioning the gain and filtering.

© IEE 2005

11 November 2004

Electronics Letters online no: 20057617

doi: 10.1049/el:20057617

Seonghan Ryu (Samsung Electronic Co., Ltd, RF Team, System LSI Division, Semiconductor Business, Giheung, Gyeonggi, Korea)

E-mail: ilikeit@postech.ac.kr

Sangsu Jin, Huijung Kim and Bumman Kim (Department of EEE, Postech, Pohang, Gyeongbuk, Korea)

Seunghyun Lee (Future Communication IC, Sungnam, Gyeonggi, Korea)

Jongryul Lee (Future Communication IC, Sungnam, Gyeonggi, Korea)

## References

- 1 Sansen, W.M.C., and Meyer, R.G.: 'Distortion in bipolar transistor variable-gain amplifiers', *IEEE J. Solid-State Circuits*, 1973, **SC-8**, (4), pp. 275–282
- 2 Otaka, S., Takemura, G., and Tanimoto, H.: 'A low-power low-noise accurate linear-in-dB variable-gain amplifier with 500 MHz bandwidth', *IEEE J. Solid-State Circuits*, 2000, **35**, (12), pp. 1942–1948
- 3 Gilbert, B.: 'The multi-tanh principle: a tutorial overview', *IEEE J. Solid-State Circuits*, 1998, **33**, (1), pp. 2–17
- 4 Coffing, D., et al.: 'A variable gain amplifier with 50-dB control range for 900-MHz applications', *IEEE J. Solid-State Circuits*, 2002, **37**, (9), pp. 1169–1175