

# A Ultra-High PAE Doherty Amplifier Based on 0.13- $\mu\text{m}$ CMOS Process

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**Abstract**—A 2.4-GHz Doherty CMOS power amplifier (PA) with ultra-high efficiency [power added efficiency (PAE)] is presented. A 0.13- $\mu\text{m}$  standard CMOS process is employed and the two-stage circuit is configured for a 3.2-V operation. For a compact realization of the circuit, all matching circuits including a quarter wave transformer and input phase compensation transmission lines are implemented with lumped components. To modulate properly and maximize the PAE at  $P_{1\text{ dB}}$ , the input power of the class C peaking power cell is adjusted by optimizing the gate bias of the peaking driver cell. By doing so, the gain compression of the carrier cell is compensated by the gain expansion of the peaking cell up to the full power. This amplifier delivers a 22.7 dBm of  $P_{1\text{ dB}}$  and 60% of PAE with 25 dB of power gain at 2.4 GHz. The PAE at 5 dB backed-off power level shows about 35%. The excellent PAE of the circuit is the best data ever reported from linear CMOS PAs. The successful demonstration of the Doherty CMOS PA with lumped components is expected to be applied for a full-integration of the circuit.

**Index Terms**—CMOS power amplifier (PA), Doherty power amplifier with lumped components, error vector magnitude (EVM), power added efficiency (PAE), third- and fifth-order intermodulation distortion (IMD3, IMD5), wireless local area network (WLAN).

## I. INTRODUCTION

THE Doherty power amplifier (PA) is one of the most prominent techniques for the power added efficiency (PAE) enhancement at a low power level [1]–[3]. The PAE at a low power level should be as high as possible for a certain communication system such as CDMA, because it is directly related to the battery life time. In the system, the most frequent signal usage happens at around 0 dBm power level. But the PAE of a normal PA for CDMA is optimized at the maximum power level, and the PAE at the low power level is comparably poor and a large portion of the battery power is consumed at this level. The Doherty configuration is also useful for the PA for a high peak to average ratio (PAR) signal. As the wireless communication is transferred into a high-speed data rate system, most of the 4G systems are based on OFDM signal. Such a signal consists of multi-carriers and each carrier transports parallel data. For example, the 54 Mbps 64-QAM signal of IEEE 802.11g WLAN

consists of 48 carrier signals and four pilot signals with PAR of over 10 dB. Therefore, to keep the integrity of the data, the PA should be extremely linear and operated at an average power level sufficiently backed-off from  $P_{1\text{ dB}}$ . The backed-off operation lowers significantly the PAE of the PA. A standard PA for WLAN normally shows about 12% PAE for OFDM WLAN at the point of error vector magnitude (EVM) 3%. Such a low PAE is not suitable for a portable wireless device. If the Doherty configuration is applied for a PA amplifying OFDM signal, the PAE of backed-off level satisfying the EVM specification can be enhanced [4]. However, the quarter-wave transmission line and input offset line for the compensation of time delay occupy a large space even if they are implemented on printed circuit board (PCB). But this problem has been solved in GaAs process [5] and the design can be adapted for a CMOS process opening a way for a high efficiency linear PA on Si.

In this letter, we report a lumped Doherty PA using standard 0.13- $\mu\text{m}$  CMOS process which has ultra high PAE. All of the matching circuits consist of lumped components and the PA is configured for a relative high 3.2-V operation.

## II. CIRCUIT DESIGN METHODOLOGY

Fig. 1 shows the basic ideal Doherty configuration. Here, the core elements of Doherty PA operation are the active load modulation, quarter-wave transmission line, and offset line for the compensation of the time delay [6]. At the input of the peaking PA, the offset line should be inserted to compensate the time delay of the quarter-wave transmission line at the output of the carrier PA. For a compact realization of the Doherty PA, the transmission lines of quarter wave transformer and offset line should be converted to lumped elements with reasonable value. As shown in Fig. 1, the quarter-wave transmission and offset lines can be implemented with low pass and high pass filter circuits consisting of lumped components. In this case, the capacitance and inductance are determined by  $C = 1/(Z_L \cdot \omega_0)$  and  $L = Z_L/\omega_0$ . Fig. 2 shows the simplified schematic of the two-stage Doherty CMOS PA with off-chip lumped components. Since the 0.13- $\mu\text{m}$  NMOS of this process has relatively low breakdown voltages of gate-oxide and drain-source, the maximum voltage swing and bias voltage are limited. Normally, the cascode connection is widely used for a high voltage operation, but the topology still has a burden of gate-oxide breakdown for the upper device and limits the drain voltage swing of the lower device, resulting in poor PAE. Therefore, for a high voltage operation, the power stage of this work employs 0.35  $\mu\text{m}$  NMOS with a high breakdown voltage on a 0.13- $\mu\text{m}$  process, sacrificing the RF power gain. The unit finger size for the power cell is selected as 5  $\mu\text{m}$  considering the nonuniform current distribution due to the high resistance of the poly gate. The number of fingers in the unit cell is selected as 30, so the total gate width of

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Color versions of Figs. 1 and 3–6 are available online at <http://ieeexplore.ieee.org>.

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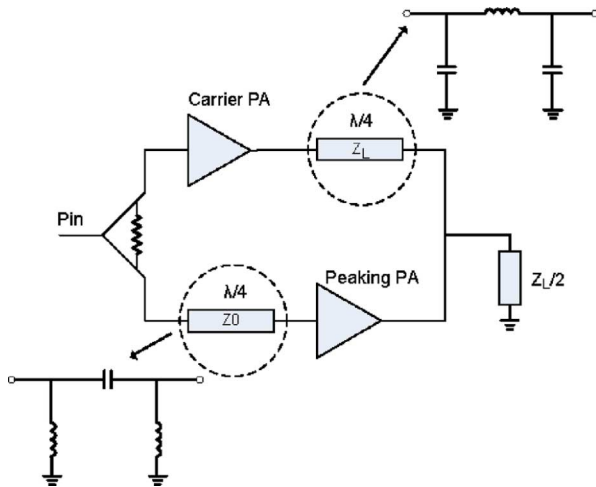


Fig. 1. Basic Doherty configuration and lumped components conversion concept.

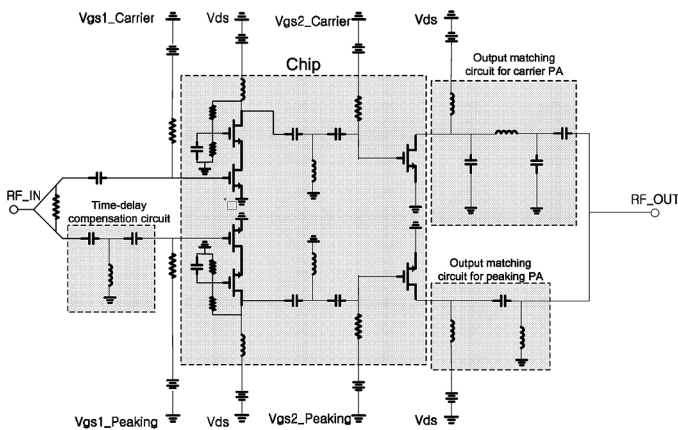


Fig. 2. Simplified schematic of Doherty CMOS PA with lumped elements.

the unit cell is  $150 \mu\text{m}$ . The power cell consists of the 12 unit cells and each unit cell is sufficiently spaced with each other to reduce thermal coupling. Total gate width of the power cell is determined through iterations of simulation to get the best RF gain and PAE. To compensate the low RF power gain of the power cells, the driver cell consists of  $0.13 \mu\text{m}$  NMOS and adopts a modified self-biased cascode configuration for a 3.2-V operation as shown in Fig. 2. The upper and lower devices consist of four unit cells whose total gate widths are  $3.6 \mu\text{m} \times 30$ . For the modified self-biased cascode stage of Fig. 2, the gate bias voltage of the upper NMOS can be adjusted, maintaining the advantages of lowering the burden of gate-oxide breakdown and hot-carrier degradation of self-biased cascode [7]. Therefore, the drain voltage swing into the hot carrier region and non-linear DCIV region can be avoided.

The  $Z_L/2$  transformer of Fig. 1 is eliminated by the direct  $50\text{-}\Omega$  power combining using  $100\text{-}\Omega$  matching cells. Thus, the output matching circuit of the carrier PA in Fig. 2 performs the load modulation from the  $100\text{-}\Omega$  and the quarter wave transmission line is converted into a low pass filter circuit. For dc bias current blocking, another capacitor is added in series with the filter circuit and the bonding wire for the dc current feeding is used as a matching inductance. Besides the impedance transformation, the output matching circuit of the carrier PA is config-

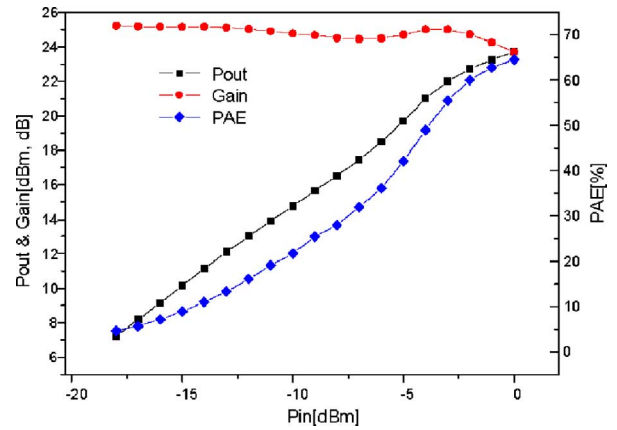


Fig. 3. Measured RF performance of Doherty CMOS PA.

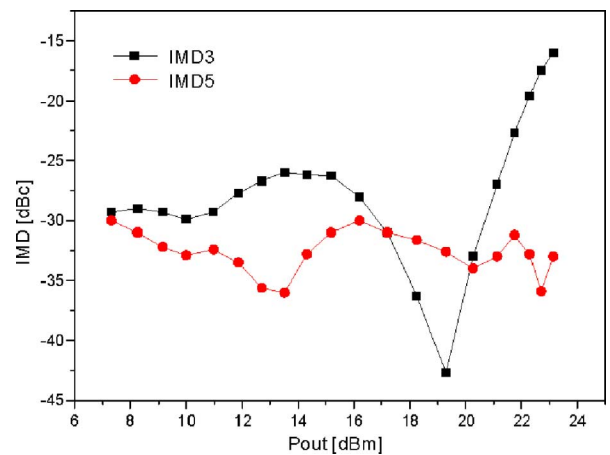


Fig. 4. Measured IMDs of Doherty CMOS PA.

ured to be resonated at  $2f_0$  terminating the second harmonics. The output matching circuit of the carrier PA should be power-matched at a high power mode. Besides, at a low power mode, the impedance of the circuit seen from the power combining junction to the output of the peaking PA should be as high as possible to prevent the power leakage from the carrier to the output of the peaking PA. Since the quarter wave transmission line is converted using a low pass filter, the time compensation transmission line of the peaking PA is realized with a high pass filter circuit, because the time delay of the high pass filter is opposite to that of the low pass filter.

Since the  $g_{m3}$  of the CMOS has positive or negative values according to the gate bias, the Doherty configuration can cancel the third harmonics generated from  $g_{m3}$  with proper biases [2]. In this circuit, the power stage of the carrier is biased at class AB and the power stage of the peaking is biased at class C. At a high power level, the ideal Doherty PA generates the maximum powers from the carrier and peaking PAs evenly. But, the class C biased peaking PA could not generate the maximum power, while the class AB biased carrier PA generates the maximum power. This is because the class C biased PA produces lower current than the class AB biased PA. Therefore, the input power for the peaking cells should be higher than that of the carrier, which is an uneven power drive [8]. By using the different gain compression and expansion according to the power level between class AB PA and class C PA, the  $P_{1\text{ dB}}$  can be further expanded

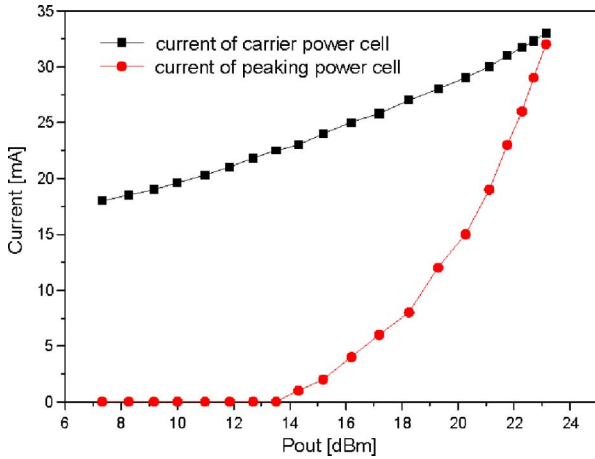


Fig. 5. Measured currents of Doherty CMOS PA.

TABLE I  
COMPARISONS OF MEASURED RESULTS

Design	Tech. [ $\mu\text{m}$ ]	Gain [dB]	$P_{out,max}$ [dBm]	PAE [%] @		
				Back-off	1dB	4dB
Sowlati [7]	0.18	36	23	18	8	4
Ding [9]	0.18	12	22	36	18	8
Heo [11]	0.18 BiCMOS	17	26	48	13	3
This work	0.13	25	25	60	38	20

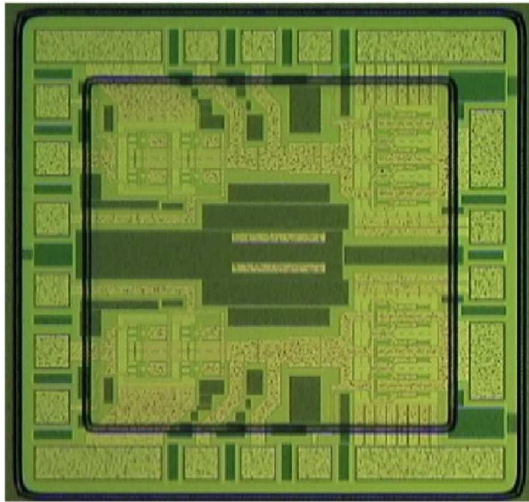


Fig. 6. Microphoto of Doherty CMOS PA.

[9], but the problem is the low gain of the class C PA. To effectively expand  $P_{1\text{ dB}}$ , the expansion curve of the peaking PA should be adjusted properly. In this work, such an uneven input power feeding is done by adjusting the gate biases of the driver cells.

### III. EXPERIMENTAL RESULTS

The lumped Doherty CMOS PA is designed for the 2.4-GHz WLAN and measured with a two-tone signal. The measured RF performances are shown in Fig. 3. At  $P_{1\text{ dB}}$ , the PA delivers 22.7 dBm and 60% PAE with 25 dB power gain. Since the OFDM signal has over 10 dB PAR, the average power of the normal linear PA should be backed off over 5~6 dB from

the  $P_{1\text{ dB}}$  to secure the EVM over 3% [10]. Fig. 4 shows the measured IMDs from the two-tone test. In this Doherty PA, the PAE at 5 dB backed-off power level shows about 35% and we expect a reasonable EVM at this point. Fig. 5 shows the measured dc currents of the power cells of the carrier and peaking part. From the figure, the current of the peaking PA around  $P_{1\text{ dB}}$  shows the same value as that of the carrier PA. This result shows that the uneven power feeding is successfully done by adjusting the gate biases of the driver cells, and the excellent PAE performance is resulted from it. In Table I, we compare this work with other CMOS PAs [7], [9], [11]. This work shows the best PAE at  $P_{1\text{ dB}}$  ever reported for linear CMOS PAs and a comparable efficiency to the switching type PA. The efficiency of the PA at 4~8 dB back-off level is highly suitable for the amplification of the OFDM signal. This CMOS PA is fabricated in a 0.13- $\mu\text{m}$  standard CMOS process. Fig. 6 shows a micrograph of the single-chip linear CMOS PA. The total chip area measures  $1 \times 1\text{ mm}^2$ .

### IV. CONCLUSION

In this letter, the successful demonstration of lumped Doherty CMOS PA is presented. The circuit of this PA is designed for an operation at 3.2 V and all matching circuits, including quarter-wave transformer and offset part for the time-delay compensation, consist of lumped components. At  $P_{1\text{ dB}}$ , the PA delivers 22.7 dBm with 25 dB power gain and 60% PAE and the PAE at 5 dB backed-off power level shows about 35%. Such an excellent PAE at  $P_{1\text{ dB}}$  is due to the uneven power feeding and the high PAE at low power level shows the successful Doherty action. This work will be a step up to the single-chip CMOS Doherty PA with high efficiency.

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