

Load modulation power amplifier with lumped-element combiner for IEEE 802.11b/g WLAN applications

J. Nam, J. Shin and B. Kim

A new monolithic microwave integrated circuit power amplifier for 802.11b/g wireless local area network (WLAN) has been implemented using the load modulation concept of a Doherty amplifier. The $\lambda/4$ transmission line for the load modulation circuit of the carrier amplifier is replaced by a lumped element based π -network, which dual functions as an output matching network, simultaneously. This amplifier shows that error vector magnitude is about 4.6% and power added efficiency (PAE) about 31.8% at P_{out} of 19 dBm for a 802.11g 64 QAM signal. PAE of the power amplifier is about 49.6%, and adjacent channel leakage ratio below 37.2 dBc at 11 MHz offset at P_{out} of 23 dBm for the 802.11b complementary code keying signal.

Introduction: Power amplifiers play a critical role in the overall performance of RF transmitter chains in WLANs and highly efficient linear amplifiers are essential for consumer applications. In general, the WLAN power amplifier operates at least 7 dB backed-off from the maximum rated power level, owing to the large peak-to-average power ratio (PAPR) of 802.11g's orthogonal frequency division multiplexing (OFDM) signal, and it can degrade the efficiency [1].

The load modulation scheme, described by Doherty, is one of the efficiency enhancement techniques and has configuration [2, 3]. The fundamental operation principle and efficiency enhancement mechanism of the Doherty amplifier has been well described previously [3, 4]. The conventional microwave Doherty amplifier is too large to be employed in power amplifier modules for mobile WLAN applications because of the $\lambda/4$ transmission line for the load modulation and additional matching network to the system impedance.

In this Letter we present a miniaturised 2.4 GHz WLAN power amplifier based on the load modulation concept using GaAs HBT technology. The $\lambda/4$ transmission line for the load modulation circuit is replaced by an equivalent lumped network, which also simultaneously functions as an output load matching network [5, 6].

Design and operation: Fig. 1 is a diagram of the load modulation amplifier implemented in this work. As shown, all components are integrated in the MMIC chip, except output matching. The $\lambda/4$ line for the load modulation is approximated by a single π -network [5, 7]. The carrier amplifier's power matching is constructed by a highpass π -network, which also functions as the load modulation network since its phase delay is the same as the quarter-wave length transmission line [6]. The highpass π -network is employed because the capacitor can function as a DC-block and the inductor can be used for a DC bias. To simplify the circuit topology and miniaturise the module, the carrier and peaking amplifiers are designed to be 100 Ω for direct match to the 50 Ω system impedance [6].

The output impedance (Z'_{aux}) of the peaking amplifier should be very high, close to an open-circuit to prevent any power loss through the amplifier path during the low input power drive. The amplifier is power matched to 100 Ω during the high input power drive. Therefore, the matching circuit of the peaking amplifier may need a two-section π -network to satisfy the above two conditions [5].

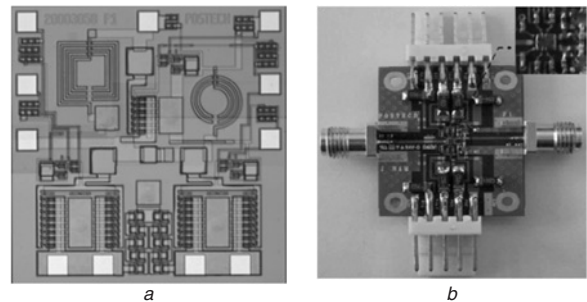


Fig. 3 Photograph of MMIC chip
a MMIC chip
b Module on test board

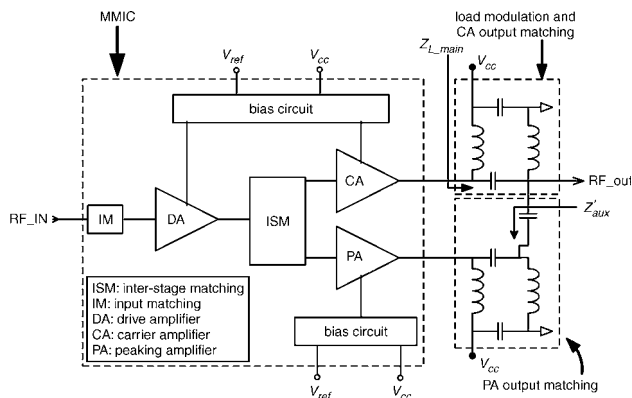


Fig. 1 Diagram of load modulation amplifier

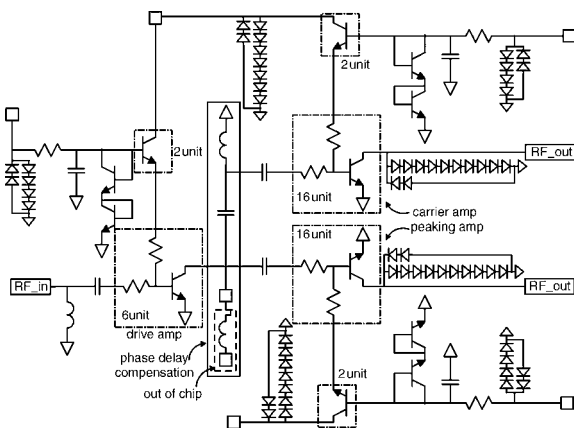


Fig. 2 Schematic of MMIC chip

Fig. 2 is the schematic of the MMIC chip designed for 802.11b/g wireless LAN (WLAN) operations. The inter-stage is integrated in an MMIC chip. This inter-stage delivers the power from the drive amplifier to the carrier and peaking amplifiers by matching to the input impedances of the two power transistors. It is constructed using a capacitor and a ballasting resistor. The inter-stage matching contains the phase delay compensation network for the phase difference due to the load modulation circuit at the output. The phase delay compensation network is implemented by a highpass π -network. The impedance of the inter-stage's combining point is designed to be matched for the optimum load impedance of the drive amplifier. The input matching of the drive amplifier and the stacked diodes to prevent electro-static discharge are integrated. The base ballasting resistor is used at each unit-cell of the power device so as to improve amplifier stability, prevent thermal collapse, and to match the network.

Photographs of the MMIC chip and module for test on a PCB board are shown in Fig. 3. The power amplifier MMIC chip is fabricated using a commercial InGaP/GaAs HBT foundry process. The power amplifier is designed using a $2 \times 20 \mu\text{m} \times 2$ finger unit-cell. Each power amplifier has 16 unit-cells and the drive amplifier contains six cells. The total chip size of the MMIC is as small as $1 \times 1 \text{ mm}$ including input matching, inter-stage matching, bias network, and ESD diodes. The output matching network is realised off-chip on the PCB board of about $4 \times 4 \text{ mm}$. The MMIC power amplifier is evaluated on an FR-4 PCB board (Fig. 3b).

Measurement results: Fig. 4a shows the RF power and linearity performances of the amplifier for 802.11g operation at 2.444 GHz with 64 QAM 54 Mbit/s signal. The total quiescent bias current is 39 mA with $V_{cc} = 3.3 \text{ V}$. The EVM of the power amplifier is about 4.6% and the PAE is about 31.8% at a P_{out} of 19 dBm. Gain varies from 22.7 to 23.4 dB in all output power ranges. Fig. 4b shows the performances of the PA for 802.11b operation with a CCK 11 MCPS signal at 2.44 GHz. The ACLR at P_{out} of 23 dBm is 37.2 dBc at 11 MHz offset with efficiency of 49.6%. Fig. 5 shows the measured spectra of this power amplifier using 802.11b/g signal sources.

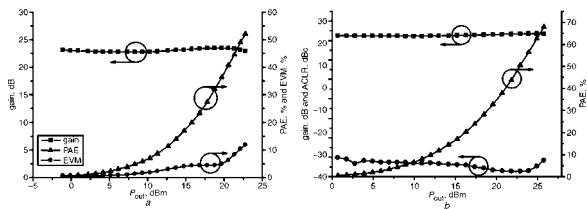


Fig. 4 RF performances of amplifier
 a 802.11g operation using 64 QAM 54 Mbit/s signal
 b 802.11b operation using CCK signal

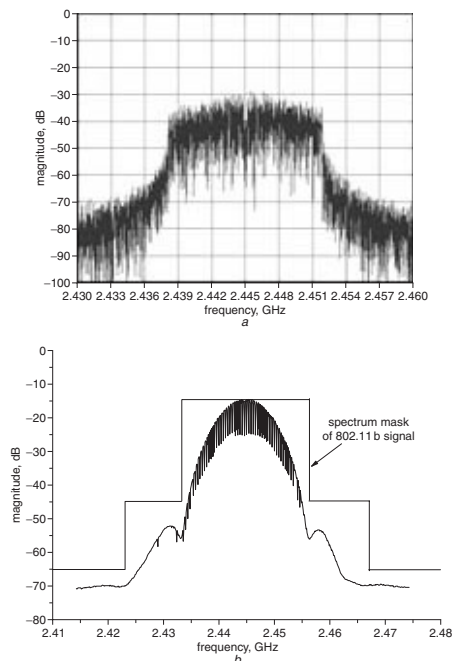


Fig. 5 Measured 802.11b/g spectra of PA
 a 802.11g 64 QAM spectrum at 19 dBm
 b 802.11b CCK spectrum at 23 dBm

Conclusion: We present a 2.4 GHz WLAN power amplifier based on a load modulation technique. The $\lambda/4$ transmission line for the load modulation circuit of the carrier amplifier is replaced by a π -network, which also functions as the output load matching network, simultaneously. The output matching networks of each power amplifier are designed for matching at 100Ω for the combined 50Ω impedance, reducing the matching components. This amplifier shows that the EVM is about 4.6%, and the PAE is about 31.8% at P_{out} of 19 dBm for the 802.11g 64 QAM signal. For the 802.11b CCK signal, the PAE of the power amplifier is about 49.6%, and the ACLR is 37.2 dBc at 11 MHz offset at a P_{out} of 23 dBm.

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