

# Memory Effect Minimization and Wide Instantaneous Bandwidth Operation of a Base Station Power Amplifier

Jeonghyeon Cha, Ildu Kim, Sungchul Hong, Bumman Kim, *Senior Member, IEEE*,  
\*Jong Sung Lee, and \*Han Seok Kim

Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang,  
Gyeongbuk, 790-784, South Korea.

\*Telecommunication R & D Center, Samsung Electronics co., LTD, Suwon, Gyeonggi, 442-742, South Korea.  
e-mail : jhcha46@postech.ac.kr

**Abstract**— We have minimized the memory effect and realized the linear amplification of a wide bandwidth signal for a next generation base station power amplifier. Using a simple nonlinear LDMOS model, the third order intermodulation distortion current is analyzed using three-dimensional power series. And the limitations in shorting the envelope and second harmonics are studied. From the analysis, we prove that the envelope is the more critical component than the second harmonic for the memory effect and linearity. In order to minimize the envelope voltages, a new matching topology is proposed, which consists of series  $L$  and  $C$  circuit for shorting the device at a low frequency while maintaining a matchable impedance at an operation frequency. The proposed power amplifier is constructed using a 90 watt PEP LDMOSFET at 2.14 GHz center frequency and tested for two-tone and multi-carrier WCDMA signals. The test results show that the memory effect and nonlinearity are drastically reduced for the proposed amplifier. For the two-tone signals, it is achieved the asymmetry of less than 2 dB up to 60 MHz tone spacing for the IMD3 and up to 40 MHz for the IMD5. For the WCDMA 20FA signal with bandwidth of 100 MHz, the linearity improvement of about 15 dB is achieved by minimizing envelope impedances. Due to the reduced memory effect, an analog predistorter could cancel the distortion by a large amount, a linearity improvement of more than 11 dB for a WCDMA 4FA signal.

**Index Terms**—Memory effect, instantaneous bandwidth, intermodulation distortion, power amplifier, LDMOSFET, predistorter.

## I. INTRODUCTION

The next generation mobile communication systems will provide a wide variety of new services, from high-quality voice, to high-definition video, to high-data-rate wireless channels. Moreover, the systems will provide combined services including the established wire and wireless communications and broadcasting networks. In order to support these services, a wide frequency spectrum will be assigned. Therefore, the base station power amplifiers of the next generation system have to cover the wide instantaneous signal bandwidth together with a highly linear amplification. But the wide-band signals may cause severe memory effects and nonlinearities in the power amplifiers [1].

The memory effects are defined as changes of the amplitude and phase in distortion components due to the previous signals. And the simplest method for characterizing them is use of a two-tone signal [1]– [4]. The two-tone signals with varying tone spacings are applied to an amplifier to measure the distortion components. If the distortion characteristics are identical regardless of the tone spacings, we can expect that the amplifier is memoryless and operate properly for the wide-band signals. Therefore, the memory effects become very important design considerations for the wide-band base station power amplifiers. Moreover, they are the limiting factor for the cancelation of distortion in linearizing an power amplifier (PA) adopting predistortion techniques [2], [5], [6]. Many previous works have tried to analyze the memory effects or reduce them [1], [4], [7], [8]. The effects are still a big problem for the current base station power amplifiers and are significant even for an amplifiers of universal mobile telecommunications system (UMTS) application, which has only a 20 MHz signal bandwidth.

The objective of this work is to minimize the memory effects of a base station PA and, further, to realize a linear power amplification of a 100 MHz bandwidth signal, which is very important for the next generation PAs. First, we have analyzed the memory effect using a simple LDMOS model [1], [9] and then the detailed simulation is carried out using Freescale's MRF5S21090 LDMOS model. The analysis and simulation show that the drain envelope impedance is the most important factor for reducing the memory effect and nonlinearity. In order to achieve our purposes, we propose a new matching topology for minimizing the drain and gate envelope impedances. The matching topology consists of series  $L$  and  $C$  for shorting the circuit at a low frequency while maintaining a matchable impedance at a operation frequency. The circuit is attached at the gate and drain terminals, rather than at the bias line, since the circuit can produce a very low impedance unlimited by the quarter wave bias line. For the experimental demonstration, based on the analysis and simulation, the power amplifier is implemented at 2.14 GHz center frequency and tested using two-tone and multi-

TABLE I  
DEFINITION OF THE NONLINEAR COEFFICIENTS FOR THE AC DRAIN  
CURRENT

$g_m$	$\frac{\partial i_D}{\partial v_{GS}}$
$K_{2g_m}$	$1/2 \cdot (\partial^2 i_D / \partial v_{GS}^2)$
$K_{3g_m}$	$1/6 \cdot (\partial^3 i_D / \partial v_{GS}^3)$
$g_o$	$\frac{\partial i_D}{\partial v_{DS}}$
$K_{2g_o}$	$1/2 \cdot (\partial^2 i_D / \partial v_{DS}^2)$
$K_{3g_o}$	$1/6 \cdot (\partial^3 i_D / \partial v_{DS}^3)$
$K_{2g_m \& g_o}$	$\frac{\partial^2 i_D}{\partial v_{GS} \partial v_{DS}}$
$K_{3_{2g_m \& g_o}}$	$1/2 \cdot (\partial^3 i_D / \partial v_{GS}^2 \partial v_{DS})$
$K_{3_{g_m \& 2g_o}}$	$1/2 \cdot (\partial^3 i_D / \partial v_{GS} \partial v_{DS}^2)$

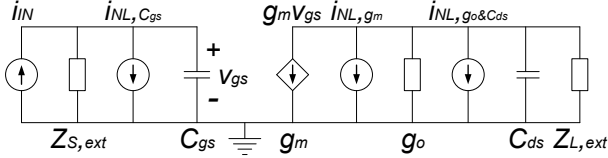


Fig. 1. FET model containing distortion current sources generated by nonlinear  $C_{gs}$ ,  $g_m$ ,  $g_o$  and  $C_{ds}$ .

carrier down-link wide-band code division multiple access (WCDMA) signals. The amplifier with the reduced envelope impedances provides drastically reduced memory effects and very linear amplification performance for wide-band signals.

## II. ANALYSIS FOR IM3

A general metal oxide semiconductor (MOS) transistor is a four-terminal device, the terminals being gate, drain, source and bulk, and the voltages in the transistor are either referred to the source or to the bulk. In the case of a laterally diffused MOS field effect transistor (LDMOSFET) used in this work, we can neglect the voltage between the source and the bulk,  $v_{SB}$ , because they are tied together. The drain current is described as a function of the gate to source voltage,  $v_{GS}$ , and the drain to source voltage,  $v_{DS}$ , and the AC drain current up to the third order nonlinear terms can be expressed by the following third order power series [1], [9],

$$\begin{aligned}
 i_d = & g_m \cdot v_{gs} + K_{2g_m} \cdot v_{gs}^2 + K_{3g_m} \cdot v_{gs}^3 \\
 & + g_o \cdot v_{ds} + K_{2g_o} \cdot v_{ds}^2 + K_{3g_o} \cdot v_{ds}^3 \\
 & + K_{2g_m \& g_o} \cdot v_{gs} \cdot v_{ds} \\
 & + K_{3_{2g_m \& g_o}} \cdot v_{gs}^2 \cdot v_{ds} + K_{3_{g_m \& 2g_o}} \cdot v_{gs} \cdot v_{ds}^2 \quad (1)
 \end{aligned}$$

where the nonlinear coefficients are defined in table I.

In order to extract the third order intermodulation distortion (IM3) level from (1), we adopt an FET model containing nonlinear  $C_{gs}$ ,  $g_m$ ,  $g_o$  and  $C_{ds}$ . We have excluded the gate to drain nonlinear capacitance,  $C_{gd}$  for simplicity of the analysis. The nonlinear components can be replaced by linear components and corresponding distortion current sources [1], [9]. The linearized model is shown in Fig. 1, which contains Norton's equivalent circuit for the input terminal and three nonlinear current sources,  $i_{NL,C_{gs}}$ ,  $i_{NL,g_m}$  and  $i_{NL,g_o \& C_{ds}}$ . Notice that the nonlinear current sources from  $g_o$  and  $C_{ds}$  are combined in one source. From Fig 1,  $v_{gs}$  and  $v_{ds}$  are written

as functions of frequency by

$$v_{gs}(w) = -Z_S(w) \cdot i_{gs}(w) \quad (2)$$

$$v_{ds}(w) = -Z_L(w) \cdot i_{ds}(w) \quad (3)$$

where

$$Z_S(w) = Z_{S,ext}(w) // \frac{1}{j\omega C_{gs}} \quad (4)$$

$$Z_L(w) = Z_{L,ext}(w) // \frac{1}{j\omega C_{ds}} // \frac{1}{g_o} \quad (5)$$

$$i_{gs}(w) = i_{NL,C_{gs}}(w) - i_{IN}(w) \quad (6)$$

$$i_{ds}(w) = g_m v_{gs}(w) + i_{NL,g_m}(w) + i_{NL,g_o \& C_{ds}}(w). \quad (7)$$

In (6) and (7), the input current,  $i_{IN}$ , has only a fundamental signal component but the nonlinear currents,  $i_{NLS}$ , have no fundamental component. If an equal power two-tone input signal is applied to the amplifier, from (1), the upper IM3 (IM3U) drain current is founded to be

$$\begin{aligned}
 i_d(2w_2 - w_1) = & g_m \cdot v_{gs}(2w_2 - w_1) \\
 & + K_{2g_m} \cdot v_{gs}(w_1) \cdot v_{gs}(2w_2) \\
 & + K_{2g_m} \cdot v_{gs}(w_2) \cdot v_{gs}(w_2 - w_1) \\
 & + 3/4 \cdot K_{3g_m} \cdot v_{gs}(w_1) \cdot v_{gs}^2(w_2) \\
 & + g_o \cdot v_{ds}(2w_2 - w_1) \\
 & + K_{2g_o} \cdot v_{ds}(w_1) \cdot v_{ds}(2w_2) \\
 & + K_{2g_o} \cdot v_{ds}(w_2) \cdot v_{ds}(w_2 - w_1) \\
 & + 3/4 \cdot K_{3g_o} \cdot v_{ds}(w_1) \cdot v_{ds}^2(w_2) \\
 & + K_{2g_m \& g_o} \cdot v_{gs}(w_1) \cdot v_{ds}(2w_2) \\
 & + K_{2g_m \& g_o} \cdot v_{ds}(w_1) \cdot v_{gs}(2w_2) \\
 & + K_{2g_m \& g_o} \cdot v_{gs}(w_1) \cdot v_{ds}(w_2 - w_1) \\
 & + K_{2g_m \& g_o} \cdot v_{ds}(w_1) \cdot v_{gs}(w_2 - w_1) \\
 & + 3/4 \cdot K_{3_{2g_m \& g_o}} \cdot v_{ds}(w_1) \cdot v_{gs}^2(w_2) \\
 & + 3/4 \cdot K_{3_{g_m \& 2g_o}} \cdot v_{gs}(w_1) \cdot v_{ds}^2(w_2). \quad (8)
 \end{aligned}$$

The lower IM3 (IM3L) current is identical but  $w_1$  and  $w_2$  are exchanged, and the  $(w_1 - w_2)$  term is complex conjugate of the  $(w_2 - w_1)$ . Among the fourteen rows of (8), the values of the first, fourth, fifth, eighth, thirteenth and fourteenth rows are not controllable by matching circuit because the in-band impedance is fixed to the optimum matching point. The values of the remaining eight rows are controllable since they are functions of the gate envelope (third and twelfth rows), gate second harmonic (second and tenth rows), drain envelope (seventh and eleventh rows) or drain second harmonic (sixth and ninth rows) voltages, which are dependant on the harmonic impedances. For convenience, hereafter, the term 'harmonic' is applied to the 'second harmonic' of  $2w_1$  and  $2w_2$  components and separated from the term 'envelope' for  $(w_2 - w_1)$  frequency component.

The memory effect is generated by the controllable terms and to reduce them, the envelope and second harmonic voltages should be reduced to zero by proper terminations. Conventionally, the short is provided at the bias line after a quarter wave transmission line. In the case, a wide-band short is difficult to be achieved since the dispersion of the line limits the achievable minimum impedance level. Thus, the

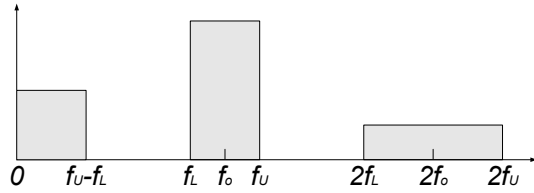


Fig. 2. Spectra distribution of the envelope and second harmonic signals.

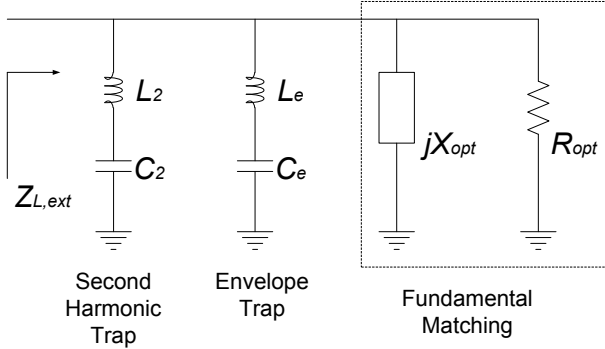


Fig. 3. Ideal output matching circuit containing the envelope and second harmonic trap circuits.

short should be provided at the gate and drain directly without passing through the quarter wave line. We have achieved the termination using a simple series  $LC$  circuit as will be shown in the following sections.

### III. OUT-OF-BAND IMPEDANCE LIMITATIONS

In this section, we investigate the realizable lower limits of the impedances at the second harmonic and envelope frequencies. This study provides the design guideline for the power amplifier with reduced memory effect.

#### A. Ideal Situations

Consider a signal with center frequency of  $f_o$  and bandwidth of  $(f_U - f_L)$ . The signal distribution is shown in Fig. 2 together with the envelope and second harmonic signals. We assume that

$$f_o = \frac{f_U + f_L}{2} \simeq \sqrt{f_U f_L}. \quad (9)$$

An ideal matching topology for the output terminal of Fig. 1 has been illustrated in Fig. 3. The input matching circuit will be identical to the output one. Figure 3 contains the envelope and second harmonic trap circuits as well as an optimum matching circuit for the fundamental signal. This circuit topology is beneficial for the termination of the harmonic voltages compared to the conventional termination at the bias line. Since the impedance dispersion caused by the quarter-wave bias line is eliminated. But the circuit adds effectively up the reactive impedance at the fundamental frequency and should be designed properly.

In order to have the impedances of the same magnitude at both frequency edges,  $2f_L$  and  $2f_U$ , for the second harmonic trap circuit,  $L_2$  and  $C_2$  have to be resonated at  $2\sqrt{w_U w_L}$ . That is,

$$L_2 C_2 = 1/4w_U w_L \simeq 1/(2w_o)^2. \quad (10)$$

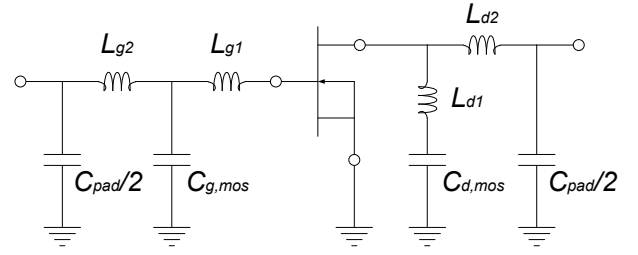


Fig. 4. Equivalent circuit for a half of the packaged MRF5S21090 LDMOS manufactured by Freescale.

If the envelope trap and fundamental matching circuits have fairly high impedances at the second harmonic frequency, the output load impedances for the second harmonics,  $Z_{L,ext}(2f_U)$  and  $Z_{L,ext}(2f_L)$ , are complex-conjugate and the magnitudes of them are

$$|Z_{L,ext}(2f_U)| = |Z_{L,ext}(2f_L)| = 4\pi L_2(f_U - f_L). \quad (11)$$

As expected, the impedances are related to the inductance and signal bandwidth.

Next, we have to use a very large capacitor  $C_e$  to short the envelope signal. Again, we assume that the second harmonic trap and fundamental matching circuits have fairly high impedances at the envelope frequency. Then the magnitude of  $Z_{L,ext}(f_U - f_L)$  is given by

$$|Z_{L,ext}(f_U - f_L)| = 2\pi L_e(f_U - f_L). \quad (12)$$

From (11) and (12), we can expect that the envelope impedance,  $Z_{L,ext}(f_U - f_L)$ , is a half of the second harmonic impedance,  $Z_{L,ext}(2f_U)$ , for the same  $L_e$  and  $L_2$  in magnitude.

Finally, the optimal fundamental signal matching is achieved by

$$-jX_{opt}(w) = (jwL_2 + \frac{1}{jwC_2}) // jwL_e // \frac{1}{jwC_{ds}} \quad (13)$$

where  $w_L \leq w \leq w_U$ . If the impedances of the envelope and second harmonic trap circuits at the fundamental frequency is extremely small, it may be impossible to match it in practice. Such a matching problem will restrict the values of  $L_e$ ,  $L_2$  and  $C_2$ . Thus the low limits of the realizable second harmonic and envelope impedances are determined.

#### B. Practical Situations

Since a base station PA designer generally uses a packaged transistor, one cannot avoid an inductive effect of bondwires between the transistor die and package lead-frame. The bond-wire inductance may give a certain advantage such as stabilization of device and increase of usable bandwidth when it is used together with an internal matching circuit. However, it will act obviously as an obstacle in controlling the envelope and harmonic impedances. In this work, we have adopted the packaged MRF5S21090 LDMOSFET manufactured by Freescale. The transistor is composed of two 45 watt cells and able to deliver a 90 watt peak envelope power (PEP). The equivalent circuit with the internal matching of a 45 watt cell is represented in Fig. 4.

At the envelope frequency, the capacitors for the internal matching can be ignored and thus the external envelope impedance is dispersed according to frequencies by just series bond-wire inductors,  $L_{g1}$  and  $L_{g2}$  for the gate and  $L_{d2}$  for the drain. Then the impedances at the envelope for the input and output,  $Z_{S,ext}(f_U - f_L)$  and  $Z_{L,ext}(f_U - f_L)$ , are given by

$$|Z_{S,ext}(f_U - f_L)| = 2\pi(L_{g1} + L_{g2} + L_e)(f_U - f_L) \quad (14)$$

and

$$|Z_{L,ext}(f_U - f_L)| = 2\pi(L_{d2} + L_e)(f_U - f_L). \quad (15)$$

On the other hand, for the second harmonic terminations, the gate and drain external matching impedances at outside of the package,  $Z'_{S,ext}$  and  $Z'_{L,ext}$ , are given by

$$Z'_{S,ext}(w = 2w_1 \sim 2w_2) = -\frac{1}{jwC_{pad}/2} // \left[ jwL_{g2} + \left( jwL_{g1} // \frac{1}{jwC_{g,mos}} \right) \right] \quad (16)$$

$$Z'_{L,ext}(w = 2w_1 \sim 2w_2) = -\frac{1}{jwC_{pad}/2} // jwL_{d2}. \quad (17)$$

(16) and (17) can be realized easily by a harmonic matching circuit including the series  $L_2C_2$  resonant circuit shown in Fig. 2 because it has a narrow fractional bandwidth contrary to wide bandwidth of the envelope signal. For the implementation of the envelope termination, a very large capacitor, such as a large tantalum capacitor, with rather small inductor should be used. The impedance level is limited by the inductors as shown in (14) and (15). Therefore, the envelope is harder to terminate than the second harmonic and the envelope components can be more important than the second harmonics in linearity as well as memory effect. In practical sense, however, we cannot guarantee that the envelope trap and fundamental matching circuits have fairly high impedances compare to the second harmonic impedance. As a result, on the envelope trap circuit, a simultaneous matching for the fundamental signal and second harmonic is needed. If the values of the internal matching components are not exactly known, it is very difficult to design the termination circuits. Thus we have optimized the circuit experimentally for a low memory effect and high linearity, focused on the envelope signal.

#### IV. SIMULATIONS

To show contributions to the memory effect from the gate and drain envelope components, Freescale's MRF5S21090 LDMOS model has been simulated using advanced design system version 2004A (ADS2004A) for two-tone signals with 2.14 GHz center frequency and tone spacings of up to 100 MHz. Figure 5 shows the circuit diagram for the simulation. In the simulation, a high voltage tantalum capacitor for the envelope trap has been selected and its scattering parameter extracted by network analyzer has been used to support the practical implementation. The tantalum capacitor has a capacitance of 10  $\mu$ F, which is large enough to short the envelope signal up to 100 MHz and also contains a parasitic frequency-dependant resistive and inductive component. The measured impedances of the tantalum capacitor are  $0.15 + j0.75 \Omega$  and

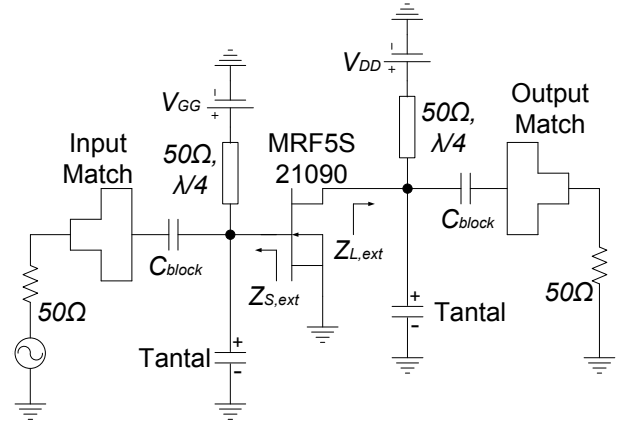


Fig. 5. Circuit diagram for the Freescale's MRF5S21090 LDMOS simulation.

$0.84 + j15.7 \Omega$  at 100 MHz and 2.14 GHz, respectively. We have utilized the parasitic inductive impedance for blocking the fundamental signal instead of  $L_e$  in Fig. 4, which is about 1.2 nH. Of course, the inductance should be resonated out by the fundamental matching circuit. It should be notice that the tantalum capacitor for the memory effect control is on the matching circuit, not on the bias line. The gate and drain bias voltages are supplied through the quarter wave transmission lines which are used to design the conventional narrow-band PA. The characteristic impedances of the lines are  $50 \Omega$  and the bias voltages are  $V_{GG} = 4.063$  V and  $V_{DD} = 27$  V, respectively. The amplifier operates in class-AB mode with the quiescent drain current of 850 mA.

In order to investigate the effect of the tantalum capacitors, the simulations have been performed for four cases, (i) case without the tantalum capacitors, (ii) case with the tantalum capacitor on the gate only, (iii) case with the tantalum capacitor on the drain only and (iv) case with the tantalum capacitors on both the gate and drain. In all cases, the input and output matching circuits have been optimized to have the same fundamental impedances,  $Z_{S,ext}(2.14 \text{ GHz}) = 2.08 - j3.54 \Omega$  and  $Z_{L,ext}(2.14 \text{ GHz}) = 2.15 - j2.0 \Omega$ , and the gain flatness within 0.2 dB over 100 MHz bandwidth and high linearities for a two-tone signal with 1 MHz tone spacing. The simulation results for the two-tone signals are shown in Fig. 6. The IMD3 (power ratio of IM3 to the fundamental signal) has been plotted according to average output powers and two-tone spacings. The output power has been swept from 30 to 46 dBm with the 1 dB division for the tone spacings of 1, 5, 10, 20, 30, 40, 60, 80 and 100 MHz. The simulation results show that the proposed PA of case (iv) has drastically reduced memory effect and improved IMD performance for all tone spacings compared to the conventional PA of case (i). Thus it is clear that the envelope component is more important than the second harmonic for the device, since we have controlled the envelope only. Also, we can obtain the following additional informations from Fig. 6.

- (1) For a narrow-band signal, the quarter wave transmission line can provide sufficient short for the envelope signal and the memory effect is not important.
- (2) For a medium-band signal, the drain envelope voltage

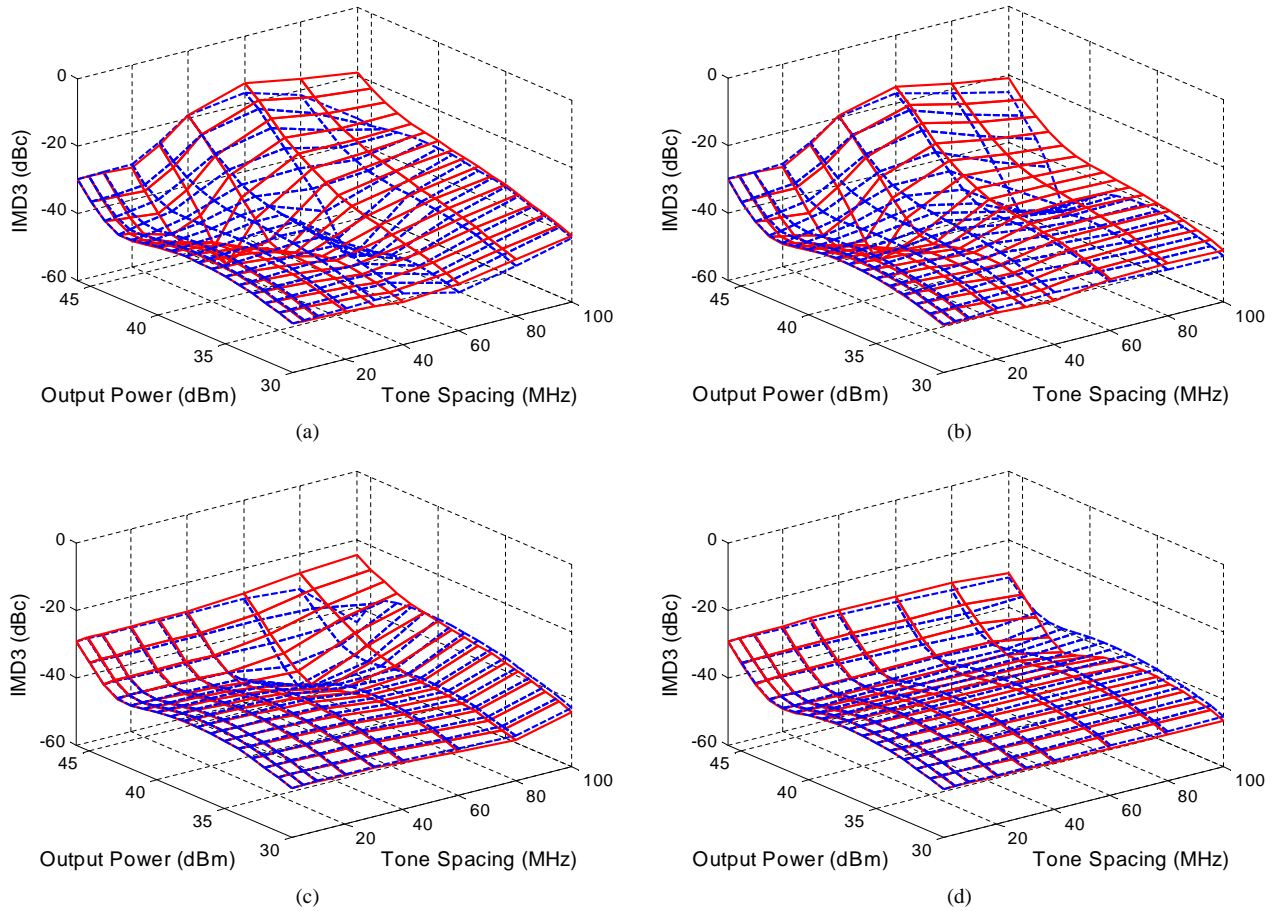


Fig. 6. Simulation results of the two-tone signals (tone spacing: 1, 5, 10, 20, 30, 40, 60, 80 and 100 MHz) for the four cases. (a) without the tantalum capacitors (the conventional narrow-band design), (b) with the tantalum capacitor on gate only, (c) with the tantalum capacitor on the drain only and (d) with the tantalum capacitors on both the gate and drain. The solid and dashed lines represent upper and lower IMD3 (IMD3U and IMD3L), respectively.

is the dominant component in memory effect and linearity.

(3) For a low power and wide-band signal, the gate envelope voltage is more important than the drain one. It may be due to the larger multiplication factor than the drain envelope.

(4) For a high power and wide-band signal, the drain envelope voltage is more important than the gate voltage but both the gate and drain envelope voltages should be controlled to reduce the memory effect and nonlinearity.

As a result, the best way is to minimize both the gate and drain envelope impedances.

## V. EXPERIMENTAL RESULTS

### A. Wideband Performance Test using Multi-carrier WCDMA Signals

For experimental demonstration, we have implemented two PAs, the amplifiers with (the proposed) and without (the conventional) the tantalum capacitors (cases (i) and (iv)) at 2.14 GHz using the MRF5S21090 LDMOS transistors and RF35 printed circuit boards. The PAs have been optimized for the similar performance in gain flatness and linearity for a down-link WCDMA 1FA signal at the same bias point,  $V_{DD} = 27$  V and  $I_{DSQ} = 850$  mA. Figure 7 shows the measured small signal gains and power spectral densities (PSD) at an average output power of 40 dBm. The drain efficiencies of the two

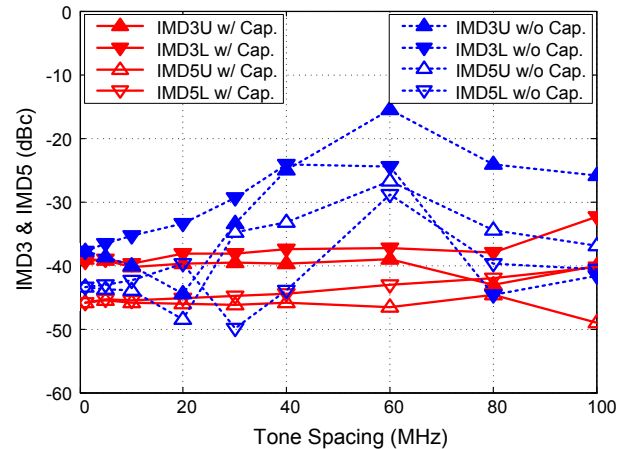


Fig. 10. Cross sectional view at 40 dBm of Figs. 8 and 9. Up and down triangles represent upper and lower IMDs, respectively.

amplifiers are nearly the same, about 18.5 % at 40 dBm. The PAs deliver flat gains within 0.2 dB over 100 MHz bandwidth and adjacent channel leakage ratios (ACLR) of about -38 dBc.

Like the simulation, the two PAs have been tested for the two-tone signal. Figure 8 shows the measured IMD3. Also we have measured the IMD5 and the measured results are

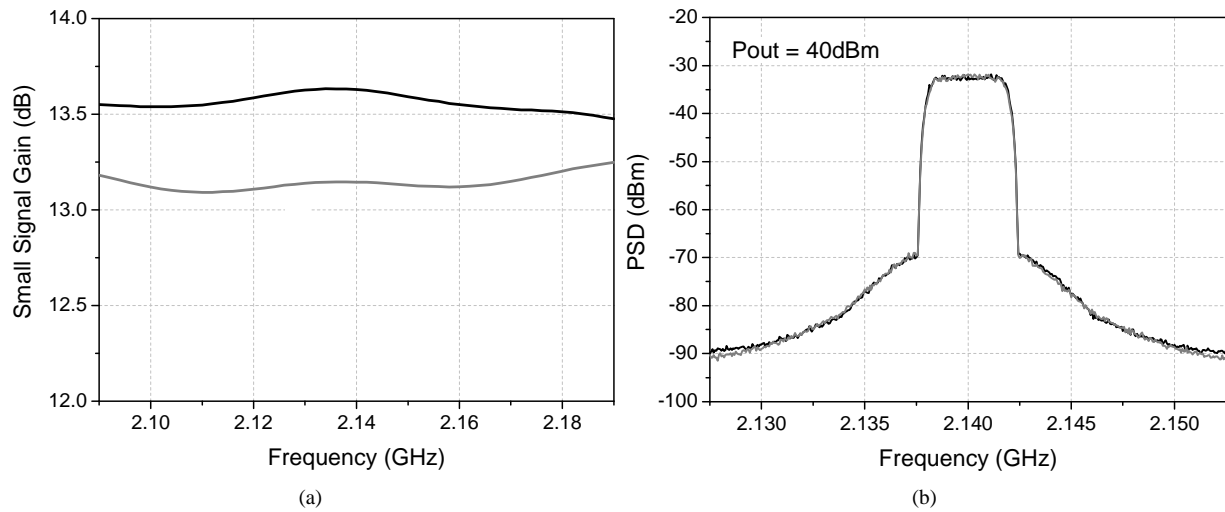


Fig. 7. The measured (a) small signal gains and (b) WCDMA 1FA spectra at 40 dBm for the conventional (without the tantalum capacitors) and the proposed (with the tantalum capacitors) PAs.

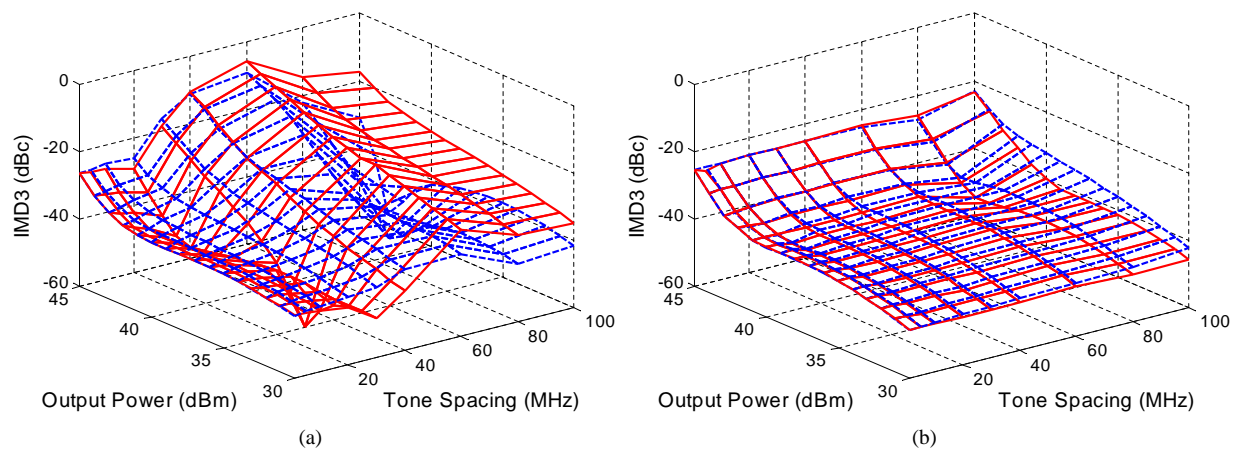


Fig. 8. The measured IMD3s for the two-tone signals (tone spacing: 1, 5, 10, 20, 30, 40, 60, 80 and 100 MHz). (a) PA without the tantalum capacitors and (b) PA with the tantalum capacitors. The solid and dashed lines represent upper and lower IMD3s (IMD3U and IMD3L), respectively.

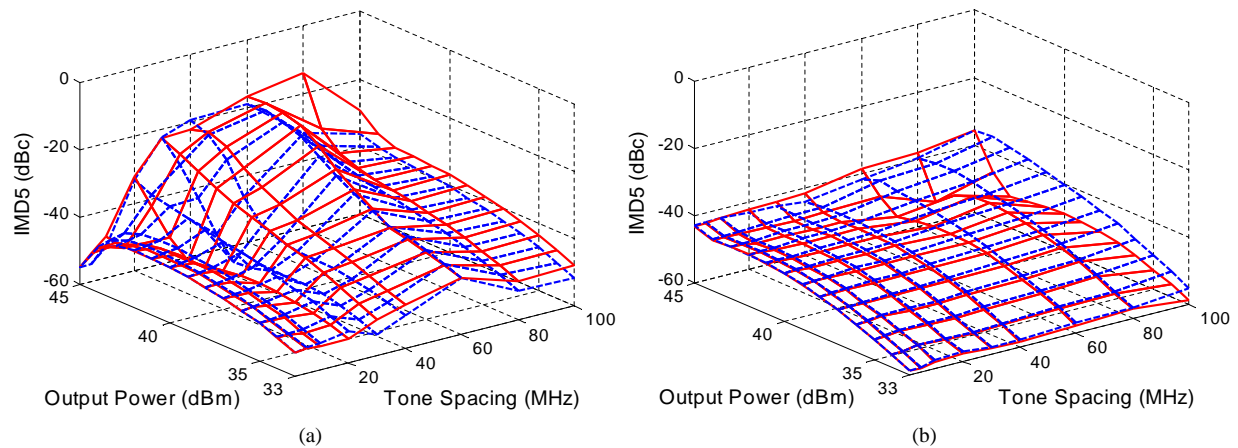
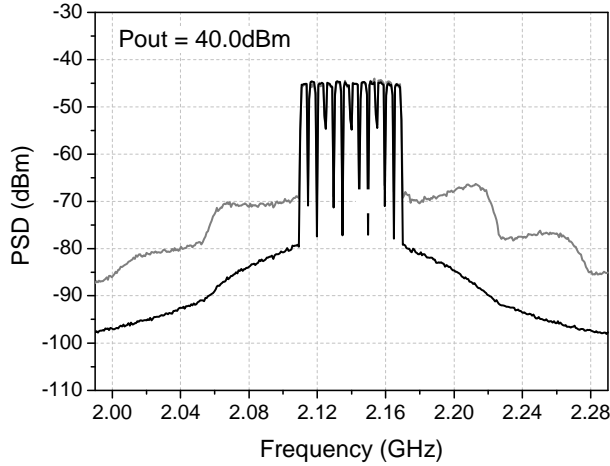


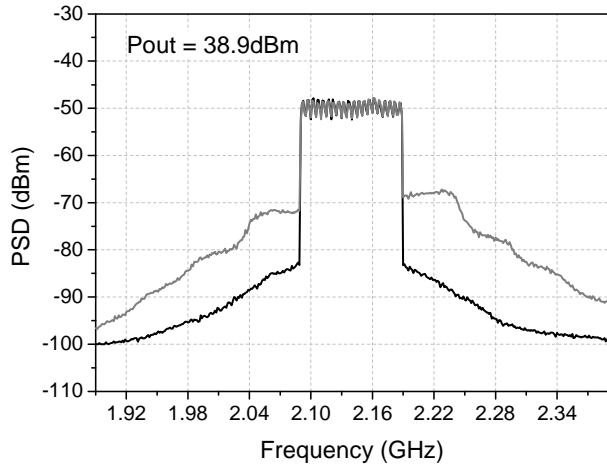
Fig. 9. The measured IMD5s for the two-tone signals (tone spacing: 1, 5, 10, 20, 30, 40, 60, 80 and 100 MHz). (a) PA without the tantalum capacitors and (b) PA with the tantalum capacitors. The solid and dashed lines represent upper and lower IMD5s (IMD5U and IMD5L), respectively.

TABLE II  
THE AVERAGE OUTPUT POWER MEASURED AT -35 dBc ACLR ACCORDING TO THE NUMBER OF CARRIER OF WCDMA SIGNAL

Number of carrier (FA)	Signal bandwidth (MHz)	Output Power (dBm)	PAR @ 0.01 % CCDF (dB) (Number of signal source (EA))
4	20	40.3	9.82 (1)
6	30	40.0	10.23 (1)
8	40	40.3	9.82 (2)
12	60	40.0	10.23 (2)
16	80	39.6	11.30 (2)
20	100	38.9	12.43 (2)



(a)



(b)

Fig. 11. The measured WCDMA (a) 12 and (b) 20FA spectra for the PAs with and without the tantalum capacitors.

shown in Fig. 9. For convenience of the view in Figs. 8 and 9, the cross sectional view at 40 dBm is represented in Fig. 10. As shown in Figs. 8–10, the proposed PA with the tantalum capacitors displays a state-of-the-art IMD performance in terms of memory effect and linearity. Especially, it has an asymmetry of less than 2 dB up to 60 MHz tone spacing for the IMD3 and up to 40 MHz for the IMD5 over all power levels.

In order to show the instantaneous wide-band performance of the proposed PA, the PA has been tested for the WCDMA 4, 6, 8, 12, 16 and 20 FA signals, which have 20, 30, 40,

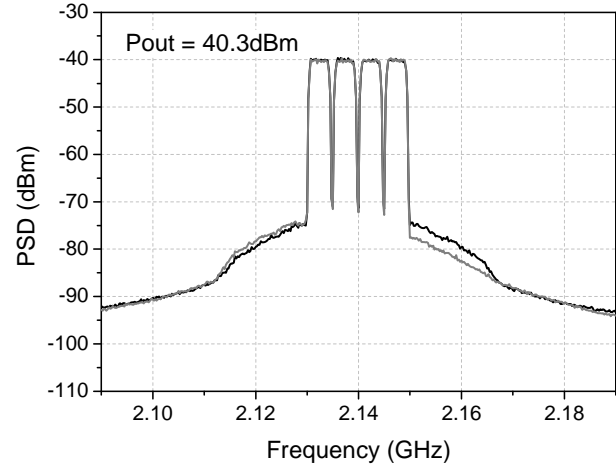


Fig. 12. The measured WCDMA 4FA spectra at 40.3 dBm for the PAs with and without the tantalum capacitors.

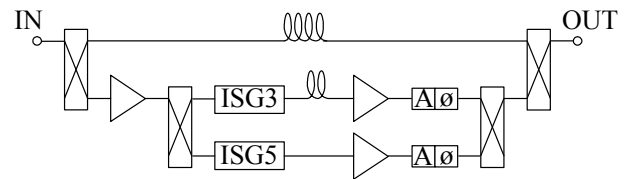


Fig. 13. Block diagram for the implemented third and fifth order analog PD. ISG3 and ISG5 mean the third and fifth order inverse signal generators, respectively, and A and  $\phi$  represent a variable attenuator and phase shifter.

60, 80 and 100 MHz bandwidths, respectively. The 4 and 6 FA signals are generated using an Agilent's E4438C signal generator and the remains using two generators. The test method is to measure the average output power at -35 dBc ACLR for the respective signals and the results are shown in table II together with the signal information. The test result shows that the performance of the proposed PA is mainly dependent on the peak-to-average power ratio (PAR) but not on the signal bandwidth. This is due to the extended instantaneous bandwidth of the PA. Figure 11 shows the measured power spectral densities (PSD) for the WCDMA 12 and 20 FA signals. For the comparison, the spectra of the conventional PA have been also displayed. The proposed PA delivers a very linear power amplification performance for a wide-band signal compared to the conventional one.

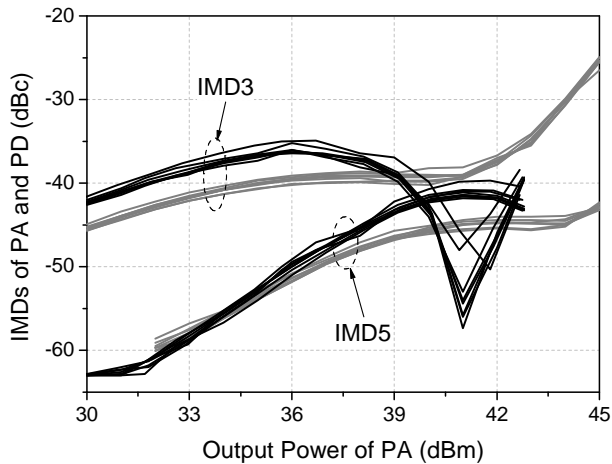


Fig. 14. The measured two-tone (up to 20 MHz tone spacing) characteristics of the PA and PD.

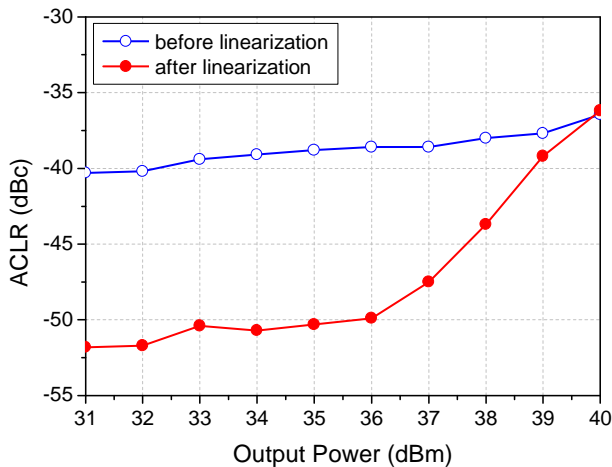


Fig. 15. The measured ACLRs for the WCDMA 4FA signal before and after linearization. The ACLR is measured at 5 MHz offset frequency from the center frequency of the uppermost or lowermost FA.

### B. Predistortion Linearization Test for Confirming the Reduced Memory Effect

In order to confirm the reduced memory effect, we have compared the output spectra of the two PAs for a WCDMA 4FA signal with 20 MHz bandwidth and linearized the proposed PA using an analog predistorter (PD). It is a good approach since the memory effect restricts mainly the linearization level of PDs. Figure 12 shows the measured WCDMA 4FA spectra, which deliver the average output power of 40.3 dBm with the ACLR of about -35 dBc. As predicted in Figs. 8–10, the proposed PA delivers a well-balanced spectrum but the conventional one does not.

We have constructed the third and fifth order analog PD to linearize the proposed PA. The block diagram for the implemented PD is given in Fig. 13 [6]. And the two-tone characteristics for the proposed amplifier and PD up to 20 MHz tone spacing are represented in Fig. 14. As shown, the IMD characteristics between the PA and PD are similar up to the output power of about 39 dBm, implying that the PA can be linearized below the power if it is memoryless [2]. Figure

15 shows the linearization result for the WCDMA 4FA signal. The PA has been linearized more than 11 dB at the average output powers below 36 dBm. If the IMD characteristic of the PD at high power levels is similar to that of the PA, a better linearization performance could be achieved at the high power levels. Nevertheless the test results are sufficient to show that the memory effect of the proposed PA is drastically reduced. Contrary to the low memory PA, the conventional PA does not produce any significant error cancelation, less than 2 dB linearization.

## VI. CONCLUSIONS

We have analyzed the IM3 component using third order power series. The envelope and second harmonic voltages create additional nonlinear components over the internal IM3 generation. The voltages are major sources of memory effect. The voltages can be eliminated by providing short at the envelope and second harmonic frequencies on the gate and drain terminals of the device. But there are some practical limits for reduced impedances. Through analysis and simulation, we have proved that the envelope voltage is more important source than the second harmonic in the memory effect and linearity. In order to minimize the memory effect and extend the instantaneous bandwidth, the envelope signals have been shorted using a large capacitor and small inductor. The inductor is practically short at envelope frequency but has a high impedance at the fundamental frequency. The circuit can be realized using a large tantalum capacitors. We have used its parasitic inductive impedance of about 1.2 nH for blocking the fundamental signal instead of using additional inductors. For the two-tone signals up to 100 MHz tone spacing, the contributions to the memory effect and nonlinearity of the gate and drain envelope voltages have been simulated according to tone spacings and power levels. The simulation results have displayed the drastically reduced memory effect and the improved IMD performance for the proposed amplifier.

For the experiment, the proposed amplifier has been implemented using Freescale's MRF5S21090 LDMOSFET with a 90 watt PEP at 2.14 GHz and tested using two-tone and down-link multi-carrier WCDMA signals. For the two-tone signals, we have found that the experimental result is similar to the simulation. For the multi-carrier down-link WCDMA signals up to 20 FA with 100 MHz signal bandwidth, the nearly bandwidth-independent linearity characteristic has been found for the amplifier. The proposed amplifier has delivered well balanced and considerably linearized spectra for the multi-carrier WCDMA signals up to 20 FA compared to the conventional one. The reduced memory effect could be confirmed by predistortion linearization test for WCDMA 4FA signal. These experimental results demonstrate clearly that the proposed power amplifier is the best performing wide-band amplifier for next generation base station applications.

## ACKNOWLEDGEMENTS

This work was supported in part by the Telecommunication R&D Center of Samsung Electronics co., LTD and the Korean Ministry of Education under BK21 project.

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