A Low Phase Noise LC VCO in 65 nm CMOS Process Using Rectangular Switching Technique

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***Abstract*—A low phase noise and low power LC voltage-controlled oscillator (VCO) has been designed using a 65-nm CMOS process. The phase noise is minimized by switching the differential core using a rectangular shaped voltage waveform, which is formed by a harmonic tuned LC tank assisted by a g_{m3} boosting circuit. The g_{m3} boosting circuit effectively maximizes the slope at the zero crossing point and reduces the transition time in which the switching transistor is operated at the triode region. The rectangular switching technique has improved the phase noise of the oscillator by 10 dB. The 450 μm $\times$ 540 μm chip consumes 4.34 mW. The proposed VCO has phase noises of -83.3, -110.7, and -131.8 dBc/Hz at 10 KHz, 100 KHz, and 1 MHz offset frequencies, respectively, from the 1.6-GHz carrier frequency.**

***Index Terms*—CMOS, harmonic tuned LC tank, harmonic tuning, low phase noise, voltage-controlled oscillator (VCO).**

I. Introduction

A MAJOR challenge in the wireless industry is the high level integration of functional blocks using low cost CMOS technology. Among the efforts for the single chip radio integration, the implementation of a low phase noise voltage-controlled oscillator (VCO) attracts a lot of attention because the phase noise of the VCO is one of the most critical parameters for the quality service of information transfer function. As the CMOS downscaling is in progress for the high level integration toward the system-on-chip at a low cost, the $1/f$ noise level of the small size transistors tends to increase, worsening the phase noise performance of the CMOS VCO. This letter presents the phase noise reduction technique of the nano-scale CMOS process. The phase noise minimization is achieved through almost rectangular shaped voltage at the switching differential cell, which is formed by a harmonic tuned LC tank assisted by a g_{m3} boosting circuit. The proposed CMOS VCO delivers a measured phase noise which is 10 dB lower than a standard one, and comparable to the LC VCO for a 0.13 μm or a larger gate length CMOS process.

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II. Circuit Design

The theory and analysis for the physical processes of the phase noise in differential oscillators [1] have progressed significantly and the techniques to lower the phase noise have advanced through the understanding of the noise mechanisms. The well-known phase noise model for an oscillator is Leeson's proportionality [2]

$$L\{\Delta\omega\} \propto \frac{1}{V_o^2} \cdot \frac{kT}{C} \cdot \left(\frac{\omega_o}{Q}\right)^2 \cdot \frac{1}{\omega_m^2}. \quad (1)$$

From this model, it can be concluded that the loaded Q of the tank needs to be maximized to reduce phase noise. Unfortunately, the integration of a high Q LC tank is not easy because of the low resistivity of Silicon substrate. In the same way, this model recommends to maximize the dissipated power in the resistive part of the resonator, which is related to the added power of the oscillator amplifier [3]. In other words, the voltage swing across the resonator needs to be maximized while minimizing the duration in the triode region of the switching transistor. To realize the concept, we have employed a harmonic tuned LC tank, which can deliver a rectangular shaped waveform voltage across the resonator [4]. The harmonic tuned LC tank boosts up the fundamental and third harmonic powers and pulls down the second harmonic power, making the output voltage waveform steeper, i.e., a rectangular shaped waveform [5]. The phase noise reduction is achieved through the almost rectangular shaped voltage at the switching cell, which effectively maximizes the slope of the switching cell output voltage at the zero crossing point. In addition, the proposed LC tank also minimizes the up-conversion of the flicker noise from the tail current source by the second harmonic short of the tank [6].

However, the harmonic tuning technique is not sufficient to maximize the slope at the zero crossing point, due to the low loaded Q of the tank that results from the low resistivity of Silicon substrate. To sharpen the voltage waveform further, a g_{m3} boosting circuit is employed. For a common-source FET biased in saturation, the output current can be expanded into the following power series in terms of the gate-source voltage (v_{gs}) around the bias point

$$i_d(v_{gs}) = g_{m1} \cdot v_{gs} + g_{m2} \cdot v_{gs}^2 + g_{m3} \cdot v_{gs}^3 + \dots \quad (2)$$

where g_{m1} is the small-signal transconductance and the higher order coefficients (g_{m2}, g_{m3}, etc.) define the strengths of the corresponding nonlinearities.

Fig. 1 shows the concept of the g_{m3} boosting circuit based on two PMOSs. The sub. transistor is used to boost up the total g_{m3} of the $I_{DS}(V_{GS})$ in order to generate high third harmonic power. Fig. 2 shows the g_{m3} boosting circuit integrated with the

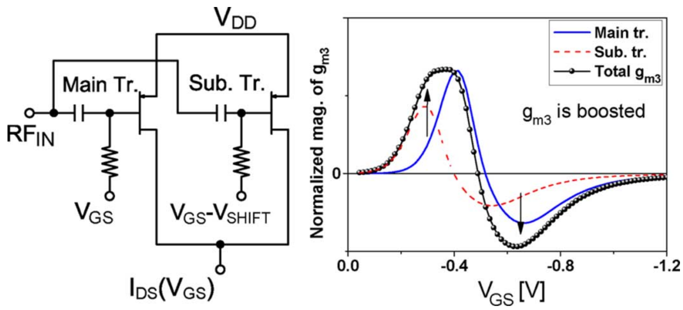

Fig. 1. g_{m3} boosting circuit.

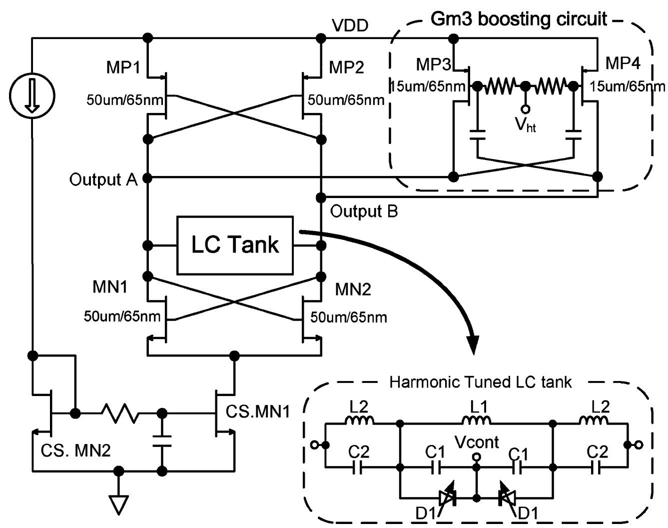

Fig. 2. Circuit implementation of the VCO with g_{m3} boosted harmonic tuned LC tank.

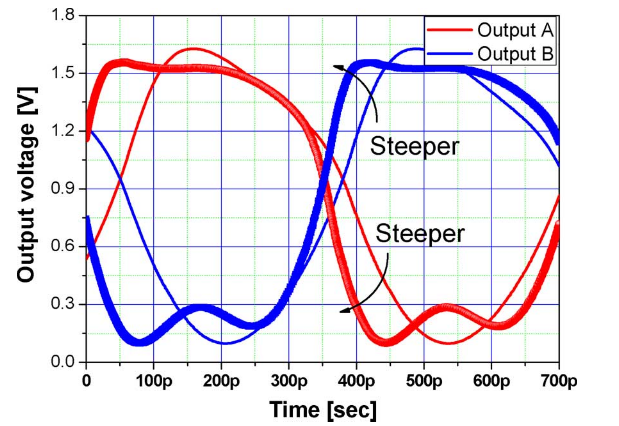

Fig. 3. Simulated output voltage waveform for the standard VCO (thin line) and the proposed VCO (thick line).

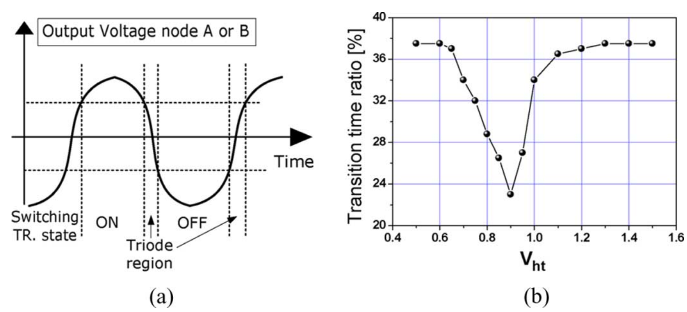

Fig. 4. Transition time ratio versus the V_{ht}.

harmonic tuned LC tank VCO. The simulated output waveform of the oscillator at the output node A and B of Fig. 2 are shown in Fig. 3. As shown, the output voltage waveform of the proposed VCO is steeper than the standard VCO at the zero crossing point. The enhanced harmonic power in the switching cell and the harmonic tuned LC tank, which enhances the impedance at the third harmonic frequency, makes the output voltage waveform steeper, i.e. a rectangular shaped waveform. Our simulation results show that the proposed harmonic tuned LC tank and the g_{m3} boosting circuit pull up the fundamental and third harmonic powers by 1.5 dB and 10 dB, respectively, while pull down the second harmonic power by 10 dB.

The total third harmonic power is a function of the V_{ht} (the PMOS gate bias, as shown in Fig. 2). The transition time ratio is defined as the ratio of the the time in which the switching transistor is fallen to the triode region to the period. The smaller transition time ratio means the steeper slope at the zero crossing time, as shown in Fig. 3. To maximize the slope at the zero crossing point for steeper transition, the transition time ratio must be minimized. To maximize the g_{m3} of the switching cell, the V_{ht} is adjusted in the moderate inversion region, as shown in Fig. 4(b). The drain current of the g_{m3} boosting circuit (MP3, MP4) is 15% of the total drain current of the current source (CS.MN1). The switching cell (MP1, MP2, MN1, and MN2) consists of the 65 nm length CMOS devices, as shown in Fig. 3. The NMOS current source has a large gate length of 1 μm for less $1/f$ noise generation from the bias circuit. In addition, the harmonic tuned LC tank must consider the parasitic capacitor of the g_{m3} boosting circuit to preserve the harmonic tuning performance.

III. Implementation and Measurement Results

The VCO shown in Fig. 2 is fabricated in a Samsung 65 nm CMOS process and tested using a HP4352S VCO/PLL signal test system. Fig. 5 shows the phase noise measurement results versus the offset frequency for the standard VCO and the proposed one. The proposed VCO has phase noises of −83.3, −110.7, and −131.8 dBc/Hz at 10 KHz, 100 KHz, and 1 MHz offset frequencies, respectively from the 1.6 GHz carrier frequency. The phase noise improvement is significant at the PMOS gate bias around the g_{m3} peak point, as mentioned in Section II. Table I summarizes the simulation and the measurement results for the proposed VCO. As shown, these measured phase noise performances and output power level show a good agreement with the simulation results except the oscillation frequency. The difference between the simulation and the measurement oscillation frequency mainly comes from the parasitic RC component of the LC tank.

Table II summarizes the performances of the standard VCO and the proposed VCO. A figure of merit (FOM) has been defined in [7] to compare VCOs performances

$$FOM = L(\Delta\omega)[\mathrm{dBc/Hz}] + 10 \cdot log\left(P_{\mathrm{DC}}[\mathrm{mW}]\right) - 20 \cdot log\left(\frac{\omega_o}{\Delta\omega}\right) \quad (3)$$

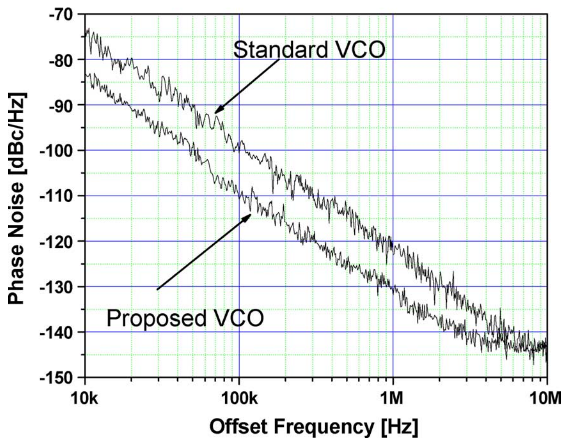

Fig. 5. Phase noise measurement results of the standard and proposed VCO.

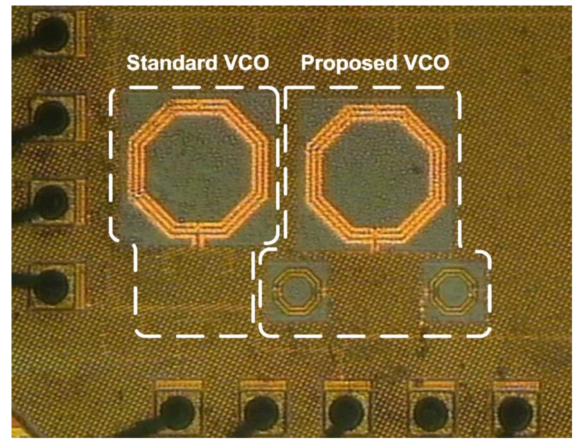

Fig. 6. Microphotograph of the VCO.

TABLE I
SIMULATED AND THE MEASURED RESULTS OF THE VCOs

VCOs	Standard VCO		Proposed VCO	
	Sim.	Mea.	Sim.	Mea.
Power [mW]	4.34		4.34	
Osc. Freq. [GHz]	1.79-2.10	1.65-1.83	1.77-2.05	1.60-1.76
P_{out} [dBm]	+2 – +3	0 – +1	+2 – +3	0 – +1
Phase Noise [dBc/Hz] @100KHz @ 1MHz	-102.1 -123.7	-100.6 -122.9	-112.5 -133.0	-110.7 -131.8

TABLE II
SUMMARY OF VCO PERFORMANCES

Parameter	Standard VCO	Proposed VCO	Ref. [5]
Phase Noise @ 10KHz @100KHz @ 1MHz	-73.0 dBc/Hz -100.6 dBc/Hz -122.9 dBc/Hz	-83.3 dBc/Hz -110.7 dBc/Hz -131.8 dBc/Hz	-74 dBc/Hz -100.4 dBc/Hz -132.0 dBc/Hz
Frequency	1.65 GHz	1.6 GHz	2.17 GHz
FOM [7]	-178.6	-188.7	-189.5
Power	4.34 mW		5.92 mW
Process	65nm CMOS		0.13μm CMOS

where $L(\Delta\omega)$ is the total single sideband phase noise spectral density at an offset frequency $\Delta\omega$, P_{DC} is total VCO power consumption, and ω_0 is the pulsation of oscillation. Even though, the switching cell consists of the 65 nm length CMOS device which has high $1/f$ noise level, the phase noise performance of the proposed VCO is comparable to the LC VCO for a 0.13 μm or a larger gate length CMOS process, as shown in Table II. The VCO core draws 2.8 mA from a 1.55 V supply. A microphotograph is shown in Fig. 6. It occupies an area of 450 μm $\times$ 540 μm.

IV. CONCLUSION

We have presented a technique to lower the phase noise of LC VCO using a rectangular voltage switching technique. Using the 65 nm CMOS devices, a low power consumption CMOS VCO is achieved. The phase noise is minimized by switching the differential core using a rectangular shaped voltage waveform, which is formed by a harmonic tuned LC tank assisted by a g_{m3} boosting technique. Even though, the switching cell consists of the 65 nm length CMOS device which has high $1/f$ noise level, the phase noise performance of the proposed VCO is comparable to the LC VCO for a 0.13-μm or a larger gate length CMOS process. The 450 μm $\times$ 540 μm chip consumes 4.34 mW. The VCO has phase noises of -83.3, -110.7, and -131.8 dBc/Hz at 10 KHz, 100 KHz, and 1 MHz offset frequencies, respectively, from 1.6-GHz carrier frequency. The results open up to the nano-CMOS processes for VCO application of wireless communication.

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