

The Doherty Power Amplifier With On-Chip Dynamic Bias Control Circuit for Handset Application

Joongjin Nam and Bumman Kim, *Fellow, IEEE*

Abstract—A monolithic-microwave integrated-circuit Doherty power amplifier (PA) with an on-chip dynamic bias control circuit for cellular handset application has been designed and implemented. To improve the linearity and efficiency in the operation power ranges, the base and collector biases of the amplifiers, except the drive amplifier of the main path, are controlled according to the average output power. The base biases are controlled using the on-chip circuit and collector biases by the dc/dc chip to reduce the average dc consumption power.

The power-added efficiency (PAE) is improved approximately 6% by the base dynamic bias control, and approximately 14% by the collector/base dynamic control from the class AB at $P_{out} = 16$ dBm, respectively. If the dc/dc converter efficiency is 100%, the PAE could be improved approximately 17.5% from class AB, reaching to 29.2% at $P_{out} = 16$ dBm. In the intermediate power level from 22 to 28 dBm, the PAE is over 34.3%. The average current consumption of the PA with the dynamic bias control is 22.5 mA in urban and 37.3 mA in suburban code-division multiple-access environments, which are reduced by 36%–46.7%, compared to the normal operation. The adjacent channel power ratio is below 47.5 dBc, and the PAE at the maximum power is approximately 43.3% in the dynamic bias operations.

Index Terms—Adjacent channel power ratio (ACPR), cellular, code division multiple access (CDMA), dc/dc converter, Doherty power amplifier (DPA), dynamic bias control, handset, InGaP/GaAs HBT, load modulation, monolithic microwave integrated circuit (MMIC), probability distribution function (PDF).

I. INTRODUCTION

RECENT MOBILE handsets for code-division multiple-access (CDMA) systems require highly linear and efficient power amplifiers (PAs) in order to maximize the standby and talk times. The PAs must be designed and manufactured to meet the output power specification of the system with maximum output of 28 dBm and ACPR under 48 dBc, while maximizing the efficiency [1]. The PAs usually deliver a high efficiency only at near the maximum rated power level, and the efficiency drops drastically as the output power level is reduced. Therefore, we can increase the talk time by reducing the average current at the low power level. The average current $\langle I \rangle$ can be defined as an integration of the product of the probability distribution function (PDF) and the current as functions of the power level, and

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The authors are with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 790-784, Korea (e-mail: pillar@postech.ac.kr).

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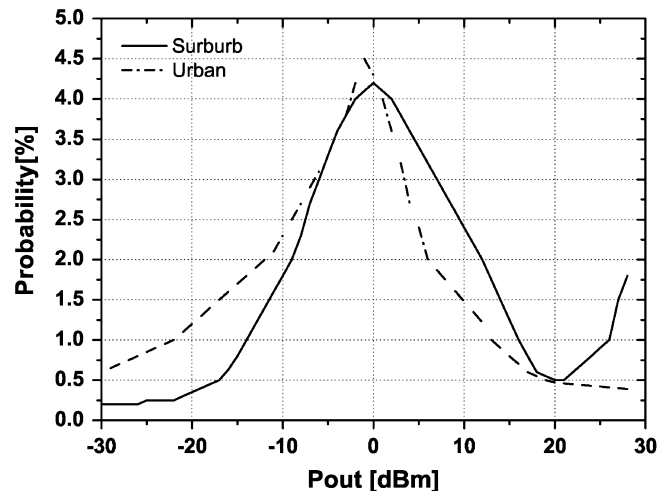


Fig. 1. CDMA urban and suburban probability density functions versus output power.

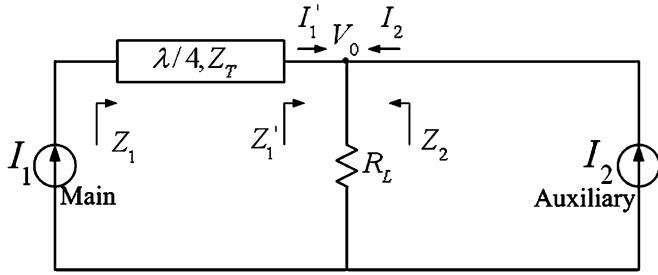
average talk time (Tt) of a handset is inversely proportional to the average current, shown as follows in (1) and (2) [1]:

$$\langle I \rangle = \int I(P) \cdot f(P) dP \quad (1)$$

$$Tt \propto \left(\int I(P) \cdot f(P) dP \right)^{-1} \quad (2)$$

Fig. 1 shows the relationship between the PDF versus the power output for a typical CDMA mobile phone [1]–[3]. Since the usual operational output power level of the PAs is far less than the maximum rated power, it is desirable to enhance efficiency at the usual operational low power level. Therefore, the techniques to achieve high efficiency at the low power level have been an important research item in handset PA design. There are many efficiency enhancement techniques at the low power level such as Kahn (envelope elimination and restoration), linear amplification using nonlinear components (LINC), bias adaptation, load modulation, and so on. The load modulation scheme, which is described by the Doherty, is the most promising solution for the handset application because it has a simpler circuit topology than others and the other techniques may degrade linearity, raise cost, and/or provide narrow bandwidth [2]–[5].

The primary method that we have taken to achieve this goal is to adjust the bias of the Doherty power amplifier (DPA) as a function of the output power level to improve the efficiency at the low power. There are four bias control methods for the CDMA PA interfacing with the baseband control integrated-circuit (IC) chip: fixed, step, logical, and dynamic biasing. The best



Where

Z_1', Z_2' : The effective impedances seen from each side of Load (R_L).

Z_1 : The Load impedance seen by the main amplifier.

Z_T : The characteristic impedance of ideal $\lambda/4$ transmission line.

I_1 : The Main amplifier's Current Source.

I_2 : The Auxiliary amplifier's Current Source.

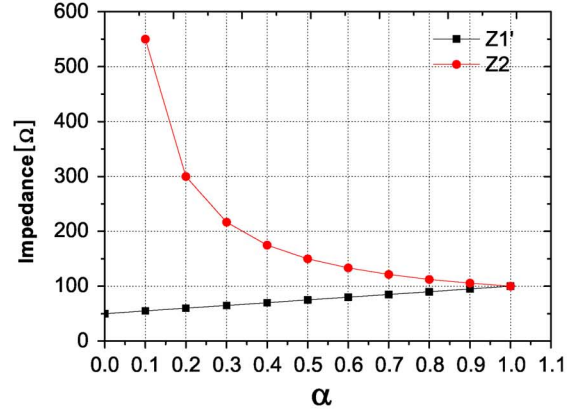
Fig. 2. Operation diagram of the load modulation circuit.

efficiency could be achieved when the bias of the PA is continually adjusted depending on the average output power level [6], [7]. The base/gate bias control is the most commonly used technique to reduce the access current at a low power level in the CDMA systems. Another bias control method is the collector/drain bias control with a dc/dc converter, which lowers the collector/drain voltage at the lower power level to improve the power-added efficiency (PAE).

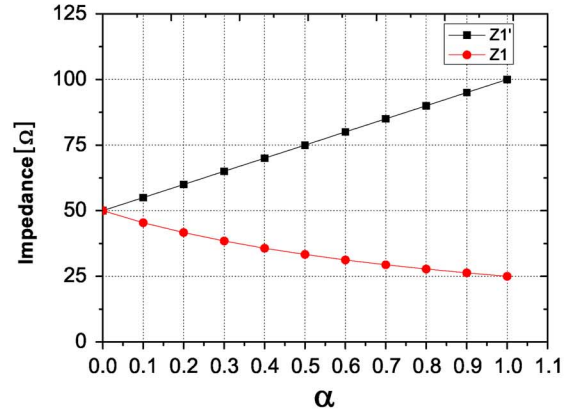
We have introduced the Doherty amplifier for handset application using lumped elements [2], [3]. The efficiency of the PAs can be boosted at the low power level using the dynamic bias adaptation according to the average output power. The base bias control circuit is integrated on the monolithic-microwave integrated-circuit (MMIC) chip, and an outside dc/dc converter is used to control the collector bias [8], [9]. The bias control circuits supply suitably low quiescent currents and voltages without sacrificing the PA's linearity at the low power level and intermediate power level, resulting in a high efficiency.

II. DESIGN AND IMPLEMENTATION OF DPA WITH DYNAMIC BIAS CONTROL

Fig. 2 shows a simplified operational diagram of the Doherty circuit, which consists of two amplifiers: namely, the main and auxiliary. Their outputs are combined in parallel through a quarter-wave transmission line, which performs the impedance transformation. The auxiliary starts to turn on as the main saturates, thereby reducing the load impedance of the main. Thus, the main can deliver more current to the load while it remains in saturation [4], [5]. Fig. 3 shows the impedances (Z_1', Z_2) seen toward the $50\text{-}\Omega$ load and both sides of the quarter-wave transmission line (Z_1', Z_1) by the variation of α , i.e., the ratio of the powers generated from the two amplifier for $R_L = 50\text{ }\Omega$, and $Z_T = 50\text{ }\Omega$ [2]. When the auxiliary amplifier is turned off, i.e., $\alpha = 0$, no power is generated from the auxiliary amplifier, the impedances of Z_1', Z_2 , and Z_1 are $50\text{ }\Omega$, ∞ , and $50\text{ }\Omega$, respectively, as shown in the Fig. 3. When the auxiliary amplifier is fully turned on, i.e., $\alpha = 1$, both amplifiers generate the same



(a)



(b)

Fig. 3. (a) Z_1' and Z_2 by the variation of α . (b) Z_1' and Z_1 by the variation of α with $R_L = 50\text{ }\Omega$, $Z_T = 50\text{ }\Omega$.

power, and the impedances of Z_1', Z_2 , and Z_1 are 100, 100, and 25 Ω , respectively, as shown in Fig. 3.

The conventional Doherty amplifier needs the quarter-wave transmission line for the impedance transformation, but MMIC implement is difficult and the line is replaced by the equivalent lumped LC network [2], [10]. A high-pass π -network is employed for the line in this study in order to supply multi-function capabilities for the elements. Fig. 4(a) shows the output matching and load modulation networks of the main amplifier. The capacitor (C_{m1}) in the high-pass π -network can function as a dc block and the inductor is used for a dc bias. The inductor in the high-pass π -network used for dc bias is replaced by a transmission line because the inductor cannot support the high dc current at a high-power region. Due to the multiple functions of the elements, we can reduce the number of matching elements, save cost, and reduce total module size. After combining the main and auxiliary outputs, an additional output matching network is needed in order to match to the system impedance level of $50\text{ }\Omega$ [11]. To simplify the circuit topology and miniaturize the module without the additional matching network, the impedance levels of the main amplifier and auxiliary amplifier (Z_1', Z_2) are designed to be $100\text{ }\Omega$ ($= 2R_L$) for direct matching to $R_L = 50\text{ }\Omega$. While one side of the high-pass π -network is designed to have $2R_L = 100\text{ }\Omega$, the other side (Z_1) is designed to have Z_{L_main} (main amplifier's optimum load impedance) by

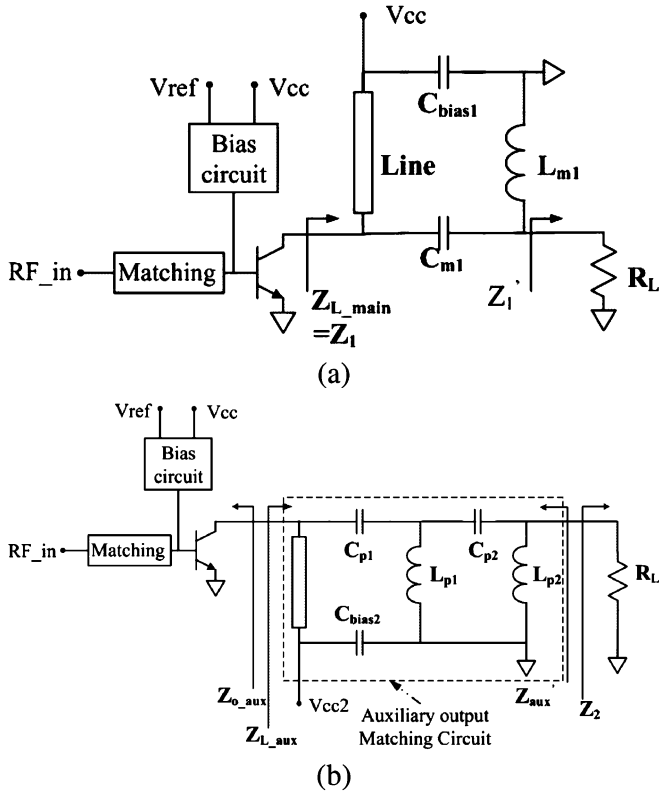


Fig. 4. Output matching schematics: (a) for main amplifier and (b) for auxiliary amplifier.

adjusting the $\lambda/4$ transmission line's characteristic impedance (Z_T) suitably, unequal to $2R_L$ (system impedance). Therefore, the lumped-element network for the load modulation can also play the role of the main amplifier's power matching network, miniaturizing the module.

There are other important design issues for the auxiliary amplifier's output load network shown in Fig. 4(b). When the auxiliary amplifier is turned off, the output impedance ($Z_{o,aux}$) of the auxiliary amplifier circuit should be high, close to open circuit to prevent any power loss through the amplifier path. When the auxiliary amplifier is turned on, both amplifiers are fully operated, and $Z_{L,aux}$ should be power matched to the auxiliary amplifier and $(Z_2)^*$ is matched to $2R_L = 100 \Omega$. The matching circuit of the auxiliary amplifier may need a multisection topology to satisfy the above two conditions. The off-state impedance is designed to be over 600Ω , which is near open compared to $RL = 50 \Omega$ [2], [11].

The input network contains the power divider to drive the two paths from one signal source. The paths for the main and auxiliary amplifiers have different phase delays because the two amplifiers' output matching networks are different. To miniaturize the power-splitter network, we use a lumped-element type Wilkinson power splitter [12]. Fig. 5 shows the input matching network to divide the input power and compensate the phase difference between the two paths. The system impedance (Z_s) is 50Ω , and Z_{inmain} and Z_{inaux} are the input impedances of the two power transistors. The output impedance of the Wilkinson divider is different from its input impedance (Z_s) for the input matching capability. The input matching networks of the two

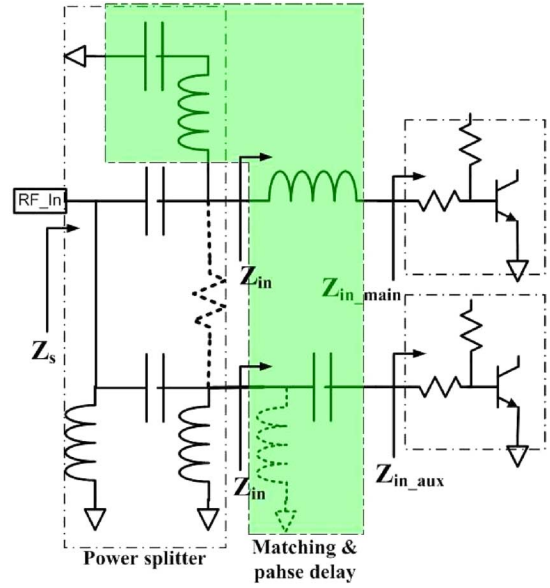


Fig. 5. Input matching and phase delay compensation schematics.

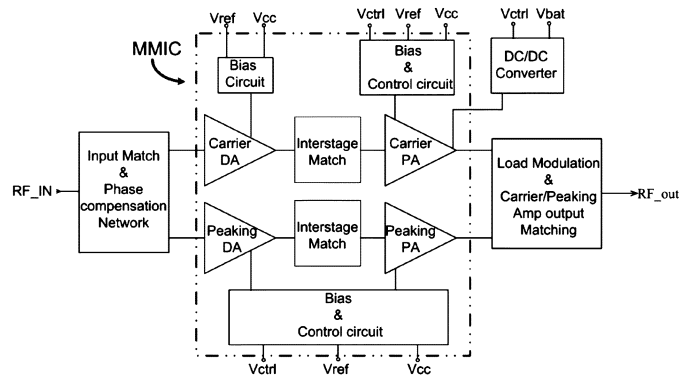


Fig. 6. Schematic diagram of the designed MMIC Doherty amplifier with dynamic bias control circuit.

chains are a low- and a high-pass network, respectively, to compensate the phase difference of the two paths, and the ballasting resistors of the devices also contribute to the input matching.

Fig. 6 shows a diagram of the MMIC Doherty amplifier with the dynamic bias control, which is designed for cellular band operation at 824–849 MHz. The main and auxiliary amplifiers consisted of two-stage PAs. The load modulation amplifier has three operation modes: low-, intermediate-, and high-power levels. In the low-power mode, the load impedance of the main amplifier is doubled by the impedance transformer, when the same size devices for the main and auxiliary amplifiers are used, because the auxiliary amplifier is open circuited. The PA's efficiency is increased due to the high load impedance. The load line of the Doherty amplifier is changed as a function of power level due to the load modulation effect, but can be further tuned by the dynamic bias control. It is difficult for the DPA to satisfy the linearity at the intermediate power level, where the main amplifier is saturated and the peaking amplifier is turned on. Therefore, the base biases are adjusted, according to the average power level, to satisfy the linearity with maximum efficiency at the intermediate power level while the drain bias

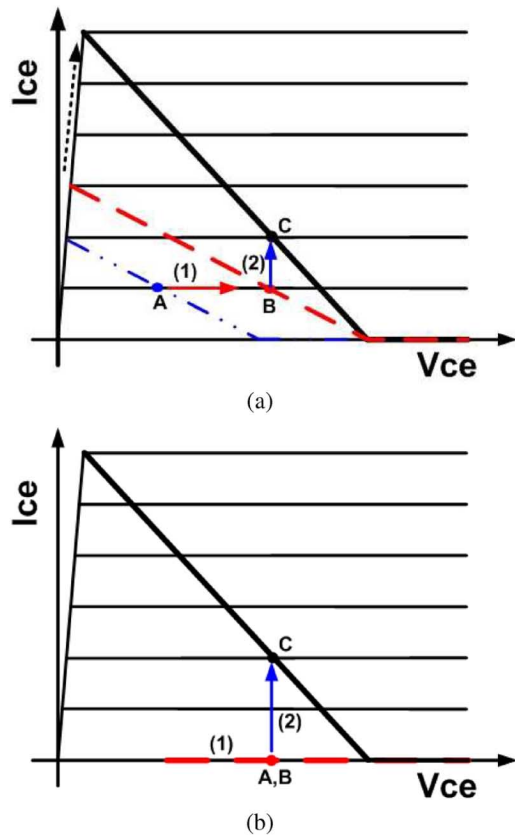


Fig. 7. Load line variation of the Doherty amplifiers. (a) Main amplifier. (b) Auxiliary amplifier.

is fixed at 3.4 V [13]. When the main starts to saturate, the auxiliary is biased at near the class AB point by the bias control circuit to satisfy the linearity, and the PAE at the power level is similar to that of the class AB. At the low power region, the collector bias is controlled while the base bias of the main amplifier is fixed. The load lines are shown in Fig. 7. We have used a dc/dc converter to dynamically control the collector bias of the main power device for the improved efficiency at a low power where only the main generates output power. Therefore, the load line is moved from point A to point B during the low power mode operation. For the high power mode, the load impedance of the main amplifier becomes the optimum power matching impedance when the auxiliary amplifier is turned on completely, and is generating the same current as that of the main amplifier. The load impedance of the auxiliary becomes the same as the main amplifier, as shown in Fig. 7. In the intermediate power mode, the power devices' load impedances are modulated, and the bias point is moved from points B to C according to the power level.

Fig. 8(a) shows the dynamic base bias control circuit. The bias is applied to all devices, except the main path's driver. Fig. 8(b) shows the node voltage and current of the bias control circuit according to the applied control voltage (V_{ctrl}). As the control voltage (V_{ctrl}) is increased, the base voltage of Tr4 (VB4) is increased by the ratio of R1, R2, and R3. When the Tr4 is turned on, the collector voltage of Tr4 (VC4) is decreased. Hence, the base voltage of Tr2 (VB2) is decreased, and the

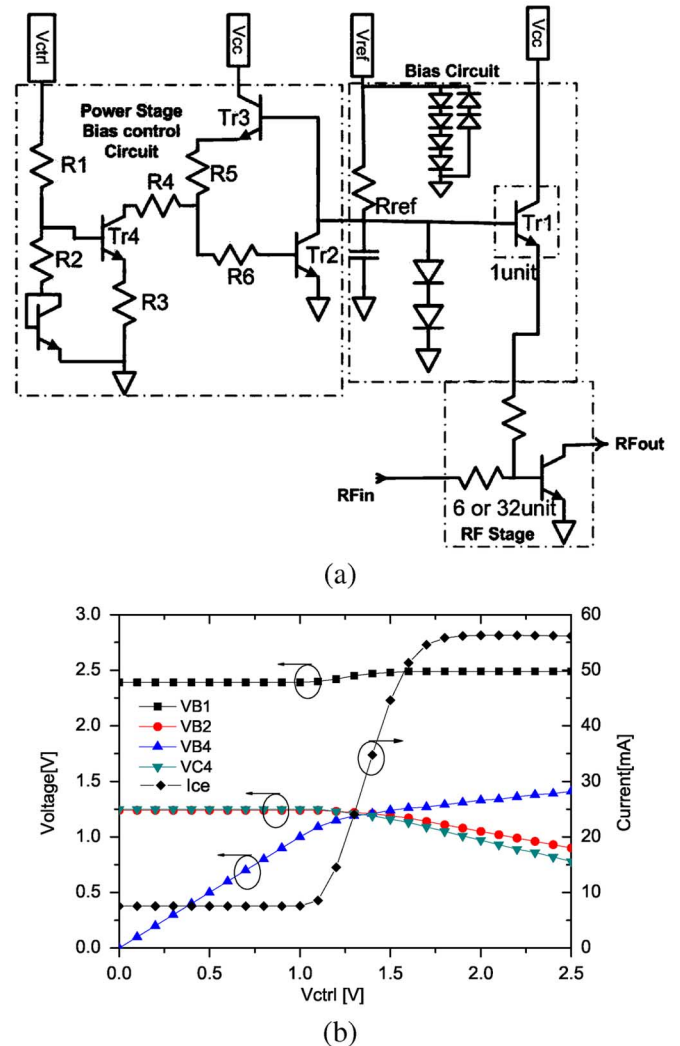


Fig. 8. Dynamic bias control circuit for the power stage. (a) Proposed dynamic bias control circuits. (b) Simulated voltage and current curves of the bias control circuit according to the control voltage.

Tr1's base voltage (VB1) is increased. The increased VB1 enhances the collector current of the power transistor (Tr1). The bias circuit's control shape can be optimized by adjusting the resistors of the bias circuit. Fig. 9 shows the control shapes of the power transistor's quiescent current (I_{ce}) versus the control voltage (V_{ctrl}) according to resistor values. When Tr4 is turned off, the initial current (I_{ce}) is determined by R5, R6, and Rref. R5 also affects the I_{ce} 's shape in the transition region. Rref is the dominant element for shaping the I_{ce} across the applied control voltage (V_{ctrl}), which is supplied from the base-band IC chip. The upper value of I_{ce} is determined by Rref and the lower value is adjusted by R5 and R6, as shown in Fig. 9. We can optimize the bias control shape by adjusting the resistors of the bias control circuit as follows. First, we determine the I_{ce} 's upper boundary using Rref within the linearity specification at the maximum power level (28 dBm). Second, we adjust the I_{ce} 's lower boundary with Rref, R5, and R6 considering the linearity specification at the low power level. Finally, the bias control voltage is shaped by R1, R2, and R3 in the midpower level, as shown in Fig. 9. This dynamic bias control circuit can be inte-

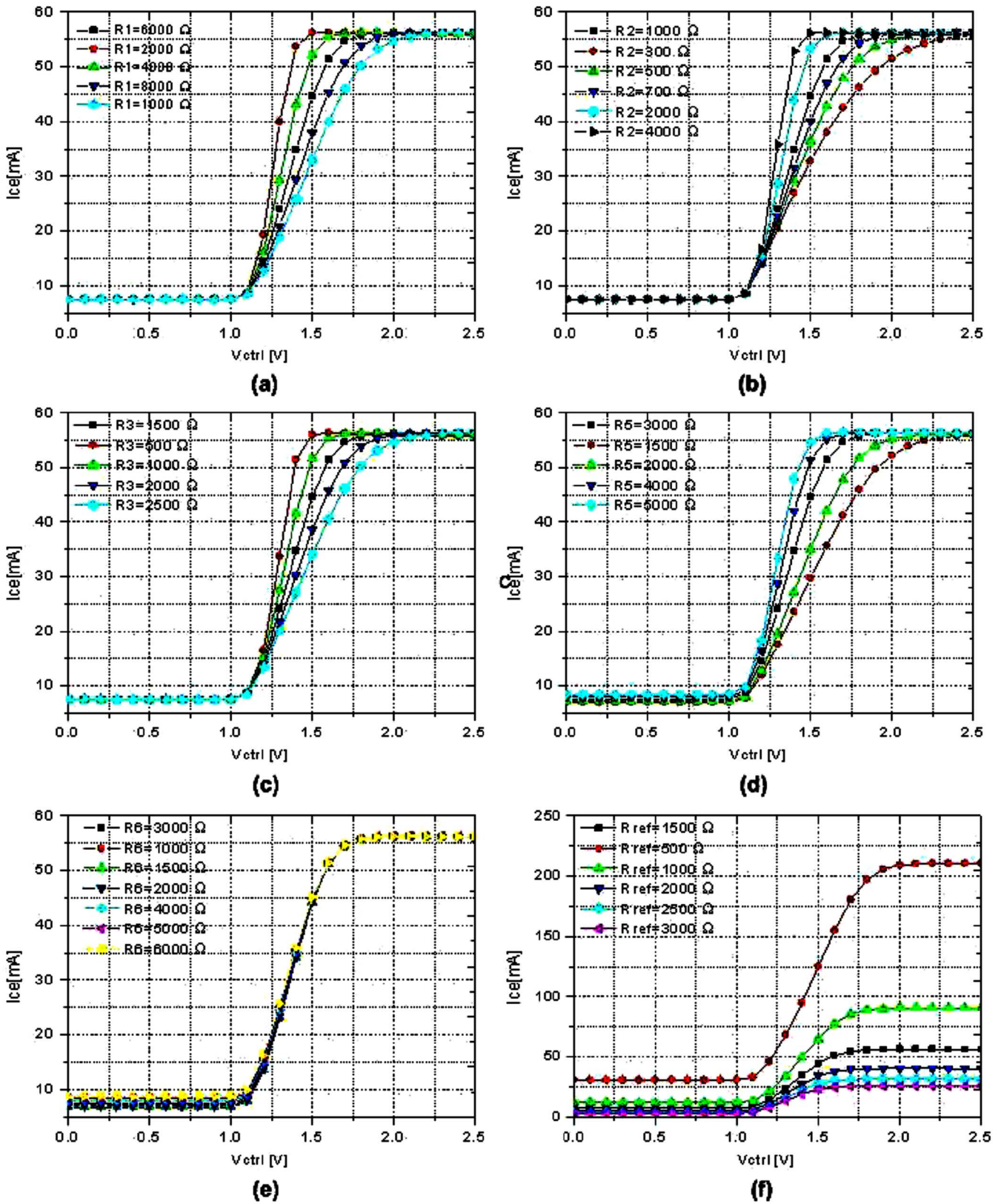


Fig. 9. Simulated RF power transistor's dc current curve according to the variation of resistances. (Initial value: $R_1 = 6000$, $R_2 = 1000$, $R_3 = 1500$, $R_4 = 1000$, $R_5 = 3000$, $R_6 = 3000$, $R_{ref} = 1500$.) (a) R_1 variation. (b) R_2 variation. (c) R_3 variation. (d) R_5 variation. (e) R_6 variation. (f) R_{ref} variation. Measured idle currents of each amplifier versus V_{ctrl} .

grated on the MMIC without increasing chip size. It adopted the control shape by adjusting the resistors according to the system

requirements, and is very simple circuitry to control the power transistor's bias current.

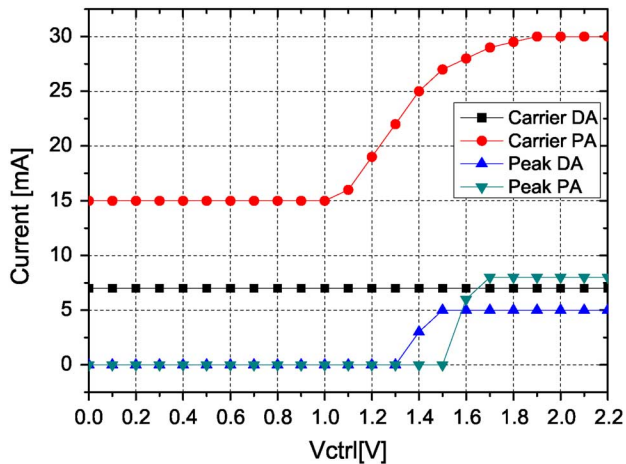


Fig. 10. Measured idle currents of each amplifier versus V_{ctrl} .

Fig. 10 shows the dc bias current's shapes of the each amplifier versus the control voltage (V_{ctrl}), which is available from the baseband controller. All the RF devices, except the main path's drive amplifier, are controlled by the bias control circuits. The main path's power stage is varied from 15 to 63 mA, the auxiliary path's drive stage is varied from 0 to 5 mA, and the power stage is varied from 0 to 8 mA. The main path's drive stage remains constant at 7 mA. These bias currents are optimized to improve efficiency at the intermediate power levels with linearity of below 48 dBc, while maintaining the collector voltage at 3.4 V. When only the main path's RF devices are operated, the commercial available dc/dc converter (MAX1820) is used to dynamically control the collector bias of the main path's power device. In this case, the efficiency of the dc/dc converter is very important and Fig. 11 shows the measured efficiency and voltage conversion shape of the dc/dc converter (MAX1820) with a 10- Ω load condition, which is close to the optimum impedance of our power devices.

Fig. 12(a) shows a photograph of the MMIC chip, which is fabricated using a commercial InGaP/GaAs HBT foundry process, and its size is as small as 1 mm \times 1 mm. Fig. 12(b) shows the full schematic of the bias controlled DPA chip. A 2 μm \times 40 μm \times 1 finger unit cell is used for the RF power device. The main and auxiliary amplifiers are two-stage, and the power stage and drive stage of the main and auxiliary paths are designed using 32 cells and six cells, respectively. The inter-stage matching network consisted of the ballasted capacitor and shunt off-chip inductor, which also work for dc blocking and dc biasing, respectively. The ballasting resistor and capacitor are inserted at each unit cell to improve stability, to prevent thermal runaway, and to match the network. The bias control circuits are also integrated in the MMIC chip and controlled by a control voltage source (V_{ctrl}), which is available from the baseband controller of a handset. Stack diodes are attached to prevent electrostatic discharge (ESD) at the output of each paths and voltage source terminals. Fig. 13 shows a photograph of the module on an FR-4 printed circuit board (PCB) for a power test. The input matching circuit, load modulation, and output matching circuits are realized on the PCB to tune the phase delay and reduce the RF output losses.

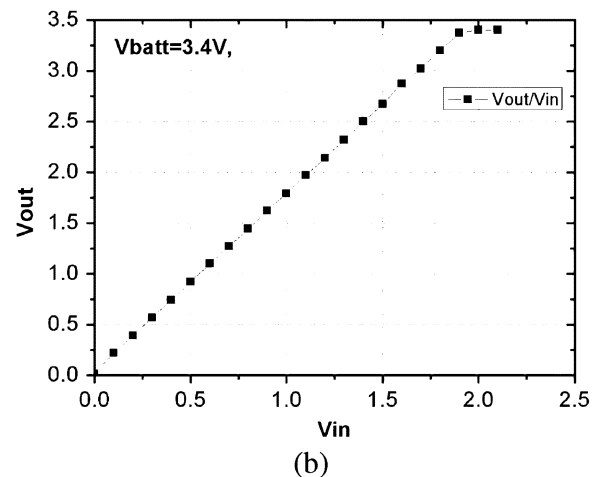
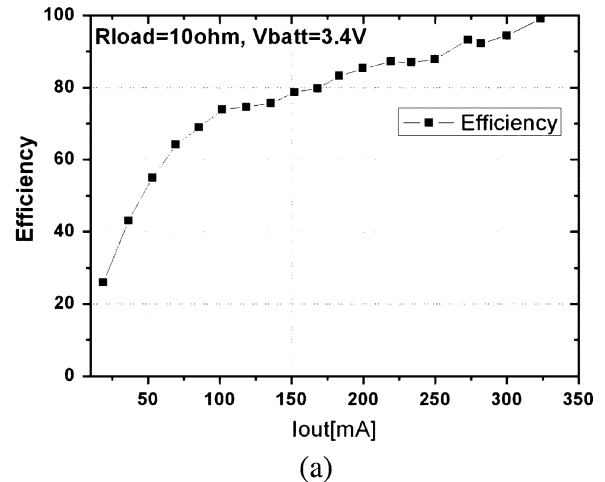


Fig. 11. Measured dc/dc characteristics. (a) Efficiency of the dc/dc converter with 10- Ω load. (b) Voltage conversion shape of the dc/dc converter with 10- Ω load.

III. PERFORMANCE

Fig. 14(a) shows measured adjacent channel power ratios (ACPRs) at 885-kHz offset versus output power for several bias conditions. The reverse-link IS-95A signal with a chip rate of 1.2288 Mc/s at 836.5 MHz. is used. When the V_{ctrl} is a fixed at 1.3 V, the ACPR is over 40 dBc around 24 dBm, and does not satisfy the CDMA specification. The ACPRs are below 47.5 dBc across all power ranges for all the other bias conditions we have tried, satisfying the commercial CDMA specification. Fig. 14(b) shows the measured gains versus output power for several bias conditions. The gains vary from 23.8 to 28.8 dB in the full dynamic control operation (LM_ V_{ctrl} _ and dc/dc), and from 26.2 to 29 dB in the base bias dynamic control operation (LM_ V_{ctrl}). The gains are 27.5 dB in the fixed bias Doherty operation ($V_{ctrl} = 1.5$ V), and 28 dB in the class AB operation (class AB). Fig. 15 shows the measured PAE versus P_{out} curves at the bias conditions. The PAE is as high as approximately 43.3% in the dynamic bias control, while it is approximately 38.4% in the class AB case at 28 dBm. When the V_{ctrl} is a fixed at 1.5 V, the ACPR is below 47.5 dBc and the PAE is improved compared to class AB, but it is lower than the dynamic bias control.

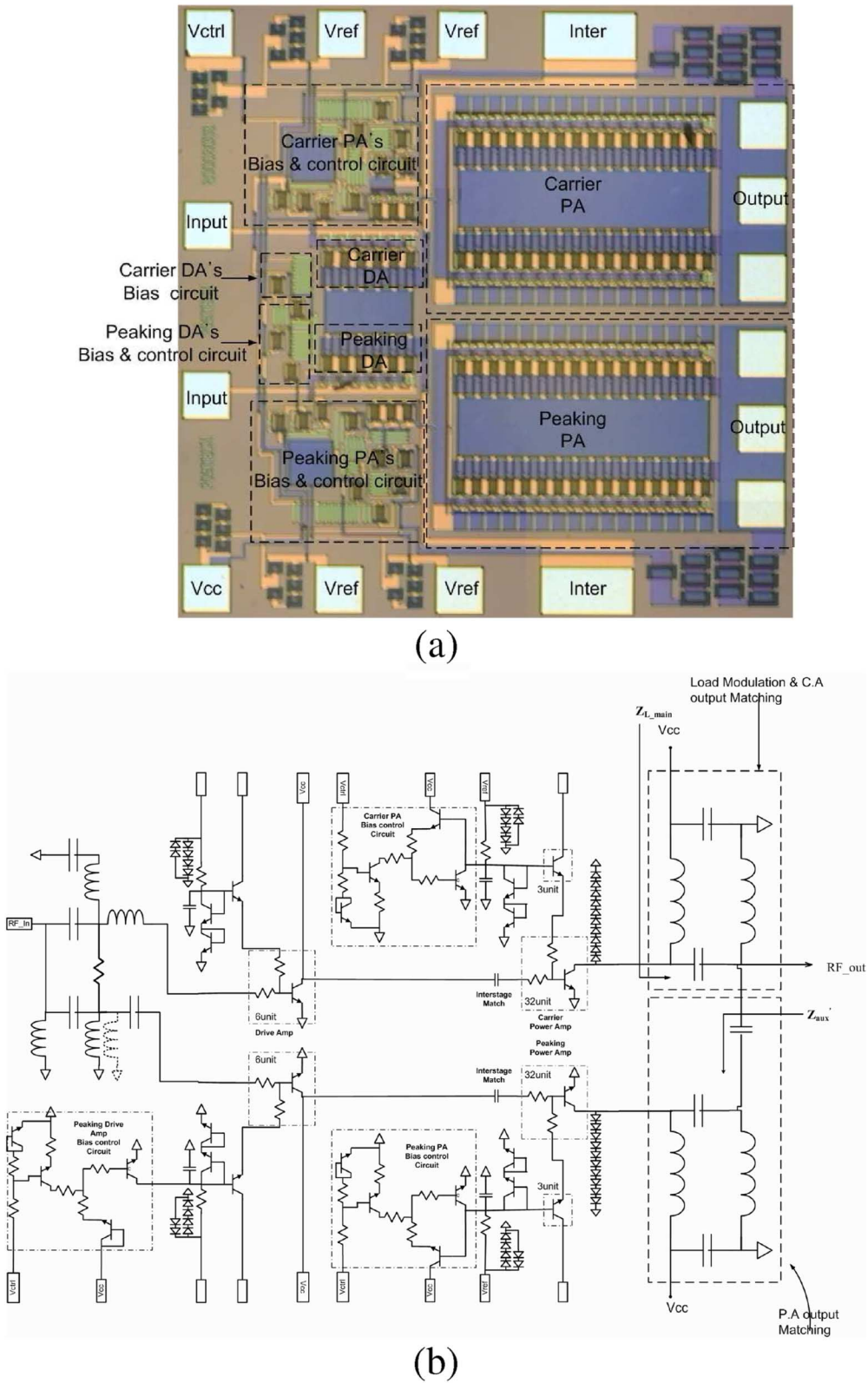


Fig. 12. Photograph and full schematic of the MMIC PA. (a) Chip photograph. (b) Full schematic of bias controlled DPA on chip.

The PAE is improved by approximately 6% by the base dynamic control, and approximately 14% by the collector/base dynamic control from class AB at $P_{out} = 16$ dBm, respectively. If the dc/dc converter efficiency is 100%, the PAE could be improved approximately 17.5% from class AB, reaching 29.2% at

$P_{out} = 16$ dBm. In the intermediate power level from 22 to 28 dBm, the PAE is over 34.3%.

Fig. 16 shows the PDF function in suburban and urban in CDMA environments, and the dc current consumptions of the PA for the bias conditions. The total quiescent bias currents are

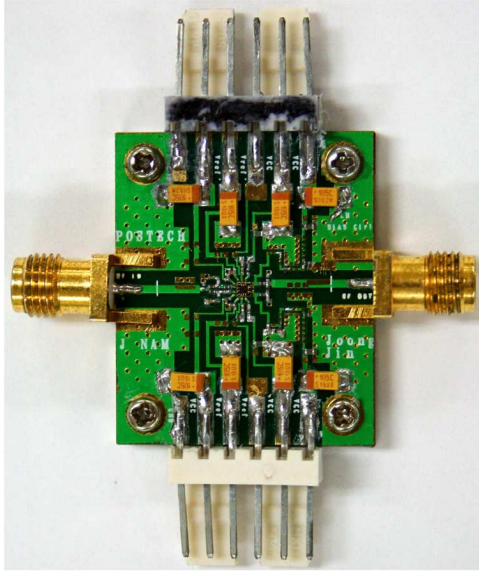
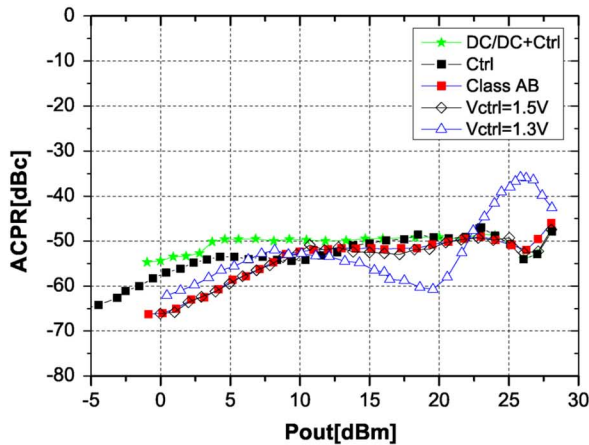
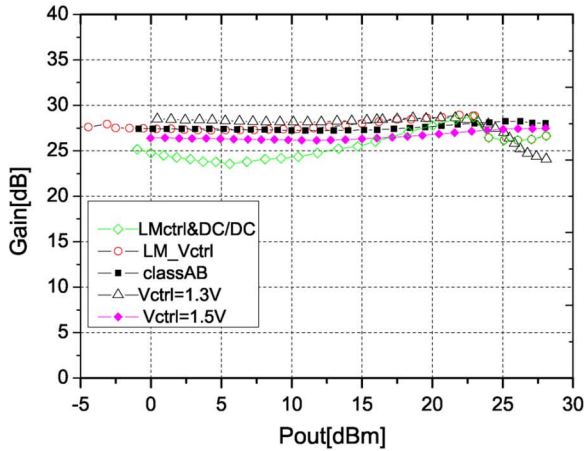


Fig. 13. Module for RF power test.



(a)



(b)

Fig. 14. RF performance of the PA for each bias condition. (a) ACPR at 885-kHz offset versus P_{out} . (b) Gain versus P_{out} .

50 mA in class AB operation, 40 mA in fixed biased Doherty operation ($V_{ctrl} = 1.5$ V), 22 mA in base bias dynamic control,

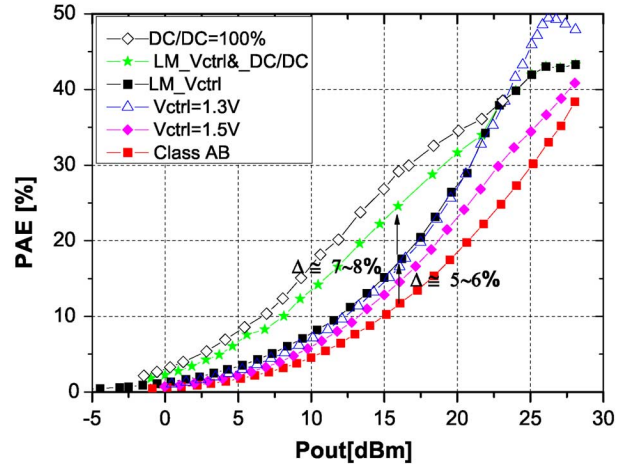


Fig. 15. PAE versus P_{out} for each bias condition.

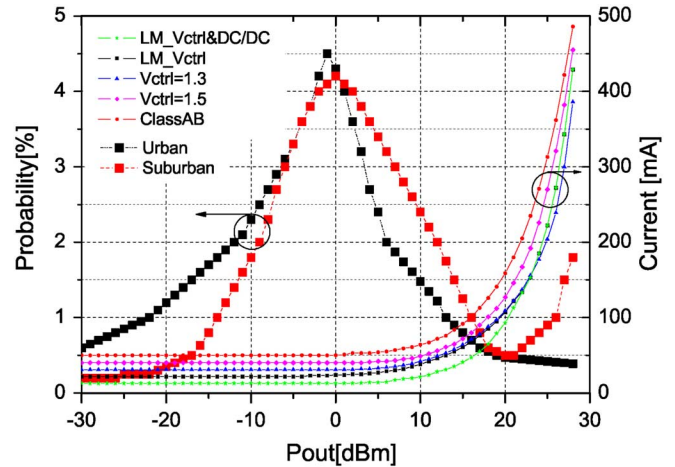


Fig. 16. PDF and dc currents versus P_{out} for each bias condition.

and 13 mA in fully dynamic bias control (base/collector bias control) operations. To evaluate the average current consumptions according to the operational bias conditions, the average currents are calculated using the PDF. Table I shows the average currents of the operations in CDMA environments. When the PA is operated in the fixed biased class AB operation, the average current is 62.4 mA in the urban environment and 79.8 mA in the suburban environment. When this PA is operated in the fixed biased Doherty operation with $V_{ctrl} = 1.5$ V, the average current is 50.1 mA in the urban environment, and 64.5 mA in the suburban environment. When this PA is operated in the dynamic base bias control condition, the average current is 33 mA in the urban environment, and 48.2 mA in the suburban environment. In the case of a fully dynamic base and collector bias control condition, the average current is 22.5 mA in the urban environment, and 37.3 mA in the suburban environment.

Therefore, the average currents are reduced from 62.4 to 22.5 mA in the urban environment and 79.8 to 37.3 mA in the suburban environment, respectively, by the bias control. The fully dynamic base and collector bias controlled DPA's average current is reduced by 36%–46.7% compared to the fixed biased class AB operation. Table II show the average currents of Doherty amplifiers with step bias control and a class AB amplifier

TABLE I
EXPECTED CURRENT CONSUMPTIONS IN CDMA ENVIRONMENTS AND
QUIESCENT BIAS CURRENTS FOR EACH BIAS CONDITION

	Expectation Current		idle
	Urban	Suburban	
LM_Vctrl&_DC/DC (dynamic)	22.5	37.3	13
LM_Vctrl (dynamic)	33	48.2	22
Vctrl 1.3 (fixed)	39.8	52.6	31
Vctrl 1.5 (fixed)	50.1	64.5	40
Class AB (fixed)	62.4	79.8	50

TABLE II
EXPECTED CURRENT CONSUMPTIONS OF THE DPA WITH STEP BASE BIAS
CONTROL AND CLASS AB PA WITH DYNAMIC BASE BIAS

	Expectation Current	
	Urban	Suburban
Doherty PA(N=3) (step)	25.8	45.3
Doherty PA(N=1) (step)	42	58.6
Class AB (Dynamic)	37.9	59.2

with dynamic base bias control, which were published in [2] and [3]. The average current of the step bias controlled DPA with size ratio $N = 1$, i.e., the main and auxiliary devices are identical, is 42 mA in the urban environment and 58.6 mA in the suburban environment, and the average current of the DPA with size ratio $N = 3$, i.e., the ratio of auxiliary device to main device, which is an extended Doherty amplifier is 25.8 mA in the urban environment and 45.3 mA in the suburban environment. The dynamic base bias controlled class AB PA is 37.9 mA in the urban environment and 59.2 mA in the suburban environment. The fully dynamic controlled DPA (LM_Vctrl_ and dc/dc) has the lowest average current consumption among the amplifiers listed in Tables I and II.

IV. CONCLUSION

It has been shown that the efficiency of a DPA for a CDMA handset can be significantly improved with the dynamic bias control circuit and, thus, the standby and talk time by lowering the expected and average current consumptions. The dynamic bias control circuits for base bias control are integrated on chip without additional costs and control the base bias at the intermediate power level, and the commercially available dc/dc converter is used to control the collector bias point of the main power device at the low power level.

We have introduced a simple base bias control circuit and have demonstrated how to optimize the control shape of the proposed dynamic bias control circuit. The proposed dynamic base bias circuits' control shape can be optimized by adjusting the resistors according to each stage's bias conditions. The measurement results show that the PAE is improved approximately 6% by the base dynamic control, and approximately 14% by the collector/base dynamic control from class AB, respectively. If the dc/dc converter efficiency is 100%, the PAE could be improved approximately 17.5% from class AB, reaching to 29.2% at $P_{out} = 16$ dBm. In the intermediate power level from 22

to 28 dBm, the PAE is over 34.3%. The proposed PA with the dynamic bias control consumes significantly less average current and improves the PAE over all of the power range. The average current consumption of the PA is 22.5 mA in the urban and 37.3 mA in suburban CDMA environments, which is reduced by 36%–46.7% compared to the fixed biased class AB operation. The ACPR is below 47.5 dBc, and the PAE at the maximum power is approximately 43.3%. The dynamic base bias controlled class AB PA is 37.9 mA in the urban environment and 59.2 mA in the suburban environment. The DPA with size ratio $N = 3$ has the lowest average current in the case of the step bias control, and the DPA has a lower average current than the class AB PA in dynamic bias control, but the fully dynamic controlled DPA has the lowest average current compared to the other amplifiers.

These data clearly show that the new amplifiers based on the load modulation with fully dynamic bias control can boost efficiency and can be a viable circuit approach for handset applications.

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Joongjin Nam was born in Uljin, Korea, in 1972. He received the B.S. degree in electronic engineering from Kwangwoon University, Seoul, Korea, in 1998, and the M.S. and Ph.D. degrees in electrical engineering from Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2000 and 2005, respectively.

From September 2005 to September 2006, he was a Post-Doctoral Researcher with the MMIC Laboratory, POSTECH. Since September 2006, he has been a Research Associate Professor with POSTECH. His

current research interests include highly linear and efficient RF PA design on the CMOS and HBT process for mobile applications, and large-signal modeling of microwave devices.



Bumman Kim (S'77–M'78–SM'97–F'07) received the Ph.D. degree in electrical engineering from Carnegie–Mellon University, Pittsburgh, PA, in 1979.

From 1978 to 1981, he was engaged in fiber-optic network component research with GTE Laboratories Inc. In 1981, he joined the Central Research Laboratories, Texas Instruments Incorporated, where he was involved in development of GaAs power FETs and MMICs. He has developed a large-signal model of a power FET, dual-gate FETs for gain control, high-

power distributed amplifiers, and various millimeter-wave MMICs. In 1989, he joined the Pohang University of Science and Technology (POSTECH), Pohang, Korea, where he is a Professor with the Electronic and Electrical Engineering Department and Director of the Microwave Application Research Center, where he is involved in device and circuit technology for RFICs. In 2001, he was a Visiting Professor of electrical engineering with the California Institute of Technology, Pasadena. He has authored over 200 published technical papers.

Dr. Kim is a member of the Korean Academy of Science and technology and Academy of Engineering of Korea. He is an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.