High-Efficiency Push–Pull Power Amplifier With High Operation Voltage

Jounghyun Yim, Ildu Kim, Daehyun Kang, and Bumman Kim, *Fellow, IEEE*

***Abstract*—A highly efficient push–pull class D power amplifier (PA) with a high operation voltage is presented. The high voltage is realized by stacking dc biases of two push–pull amplifiers through the virtual ground point, while the radio frequency powers are series combined. The drain supply voltage is increased to 44 V, which is double of the rated bias voltage (22 V) of the active devices. The LDMOS PA provides an output power of 40.6 dBm with a power-added efficiency (PAE) of 58.7% at 836.5 MHz. Each push–pull amplifier provides 38-dBm output with a PAE of 64%**

***Index Terms*—Class D, power amplifier (PA), push–pull, stack-up.**

I. Introduction

FOR biasing of a power amplifier (PA), a dc–dc converter is generally used to change the power supply voltage to the required bias voltage of the amplifier. To get the same amount of output power, the PA with a low operation voltage must handle a large current. The large current increases parasitic losses in the matching networks, transistors, and bias circuits. The losses degrade the power-added efficiency (PAE) of the amplifier. Therefore, it is preferred to increase the operation voltage of the amplifier. Also, the scale-downed CMOS transistor operates at a low voltage and a means to operate at a high supply voltage, usually 3.3 V, is needed.

There are several reports to increase the operation voltage of an amplifier, higher than the rated voltages of the active devices [1]–[3]. One method is the cascode configuration [2]. Although, the operation voltage can be increased a little by the configuration, the power performance of the circuit is degraded due to the loss in the common gate stage. Another method of increasing the voltage is stacking up the dc bias while parallel combining the radio frequency (RF) powers [1]. Some simple solutions exist for the circuit at millimeter-wave band applications.

The dc bias stack-up circuits with the isolated RF swings are formed using large capacitors, quarter-wave length transmission lines, and/or large inductors. At low frequency application cases, the quarter wave length line is too long and the large inductor or capacitor is too big to be integrated. Moreover, the powers are parallel combined.

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The authors are with the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Gyeongbuk 790-784, Korea (e-mail: im1004@postech.ac.kr).

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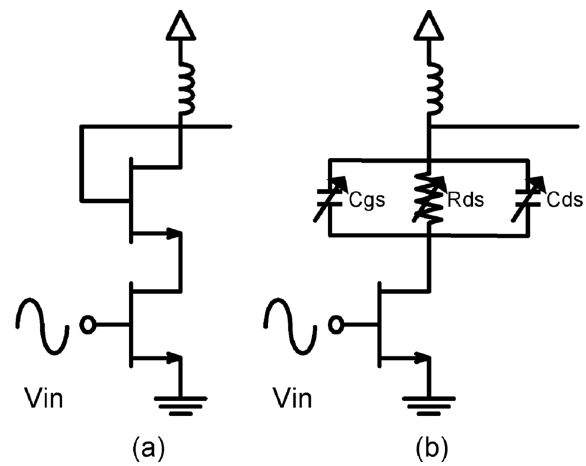


Fig. 1. Cascode circuit topology: (a) simple cascode and (b) cascode model.

In this work, we have demonstrated a new high operation voltage PA topology which does not have any deteriorative effects.

II. PA With High Operation Voltage

The cascode topology is widely used to increase the drain bias voltage and output power. Fig. 1 shows the cascode configuration. To increase the operation voltage, various methods of biasing the common-gate transistor have been developed and many analyses have been made [2]. But, the common-gate transistor of the cascode doesn't work as an active amplifier, instead it works as a parallel connected nonlinear resistor and nonlinear capacitors as shown Fig. 1(b). The structure can support a higher voltage swing, but the power loss through the common-gate transistor degrades the total efficiency. To use all dc supply for the amplification function, the common-gate transistor of the cascode circuit must function properly for the power amplification. Fig. 2 shows the full cascode circuit with proper input. Fig. 2(a) is a simple cascode connection with identical input. In this case, the upper device's source is not common RF grounded and it doesn't work properly because V_{gs} does not follow the input signal swing. If a large value inductor is used as an RF choking inductor and a large value capacitor is used as an RF short as shown Fig. 2(b), the upper device's source is RF grounded and it functions properly with a double supply voltage [1].

In the millimeter-wave applications or circuit applications whose size is not a big problem, the large inductor can be replaced by a quarter wave length transmission line. In the RF monolithic micorwave integrated circuit (MMIC) applications, the quarter wave length transmission line, large inductor and

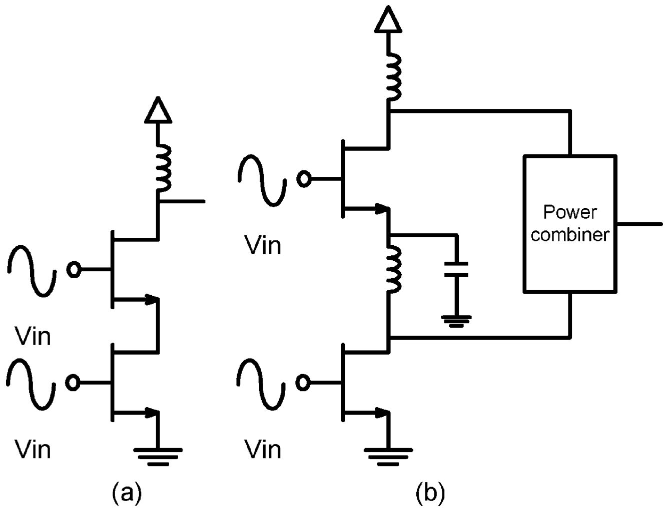


Fig. 2. Simple cascode circuit with proper input. (a) Simple connection. (b) Series connection with RF choke Inductor and shunt short capacitor.

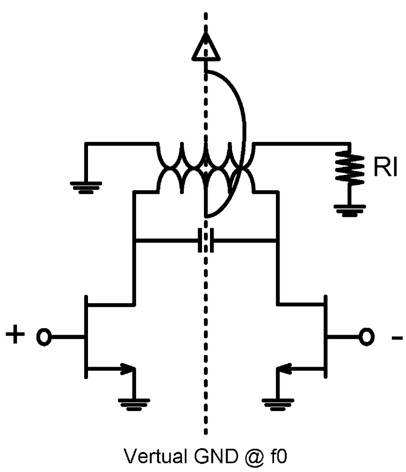


Fig. 3. Push–pull with transformer.

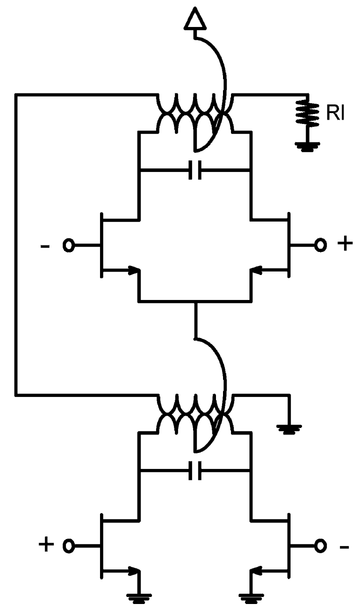


Fig. 4. Stacked-up push–pull amplifier.

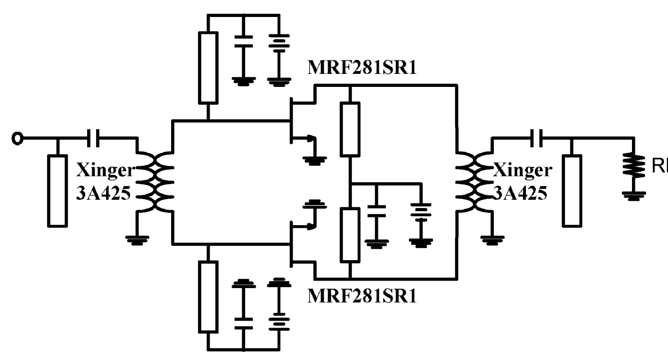


Fig. 5. Schematic of the push–pull PA.

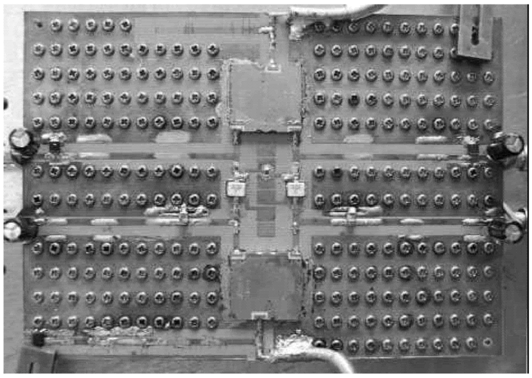
capacitor are too big to be integrated. Since the integrated inductor is very resistive, the inductor generates dc power loss and it would degrade the efficiency. The circuit has two problems of bias connection circuit using inductor and parallel power combining.

The topology shown in Fig. 3 is a push–pull PA which uses a transformer to combine the output power. It operates for the balanced signal, and there is a virtual ground at the symmetrical center line [4], [5]. At that point, odd order signals are canceled and there are only dc and even order signal components. It provides a perfect bias inject point for the stack up operation.

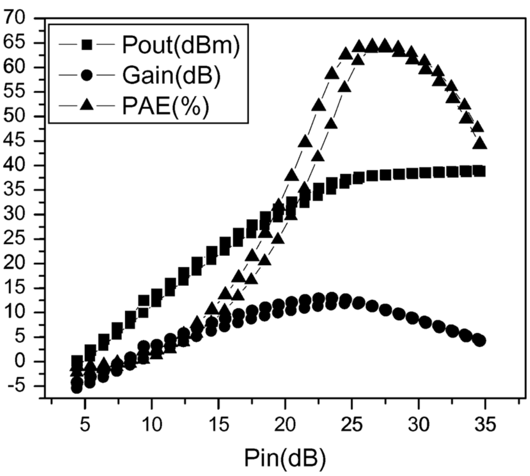
In Fig. 4, the two push–pull PAs with a virtual ground, which is shown in Fig. 3, are stacked up in dc through the virtual ground to operate at a high dc supply voltage and the RF powers are series combined solving the two problems. In the topology, the even order signals in the bias current paths produce some even order harmonic components at the output, but it can be filtered out at the output matching networks. Due to the series voltage combining nature, the current level is low and the parasitic circuit loss can be reduced, raising the efficiency. The topology doesn't use RF choking inductor or grounding capacitor and the miniaturized low loss transformers are available [6], [7]. Therefore, the proposed topology can be very useful for integrated PA with high operation voltage.

III. Design and Experimental Results

To demonstrate the stacked push–pull amplifier, the push–pull PAs are designed at 836.5-MHz band using Freescale LDMOSFET MRF281SR1 whose bias conditions are 3.4 V at the gate and 22 V at the drain. The class D amplifier is designed using Agilent's Advanced Design System with Freescale RF high power model. The chip baluns of Xinger 3A425 are used for the input and output transformers. Fig. 5 depicts the designed push–pull PA schematic. To realize a compact size, the in-out ports are matched with only one capacitor and one open stub, besides the bias lines also function as a short stub for the internal matching. The series connected capacitor and the parallel connected stub before the load play the role of a series connected capacitor and inductor for the odd harmonic tuning. Because the chip balun of Xinger 3A425 has no additional pin for the virtual ground connection, two drain bias lines are connected to have a virtual ground.



(a)



(b)

Fig. 6. Push–pull PA and the test results (a) fabricated push–pull PA and (b) test results of two push–pull PAs.

We have measured output powers and PAEs of the two amplifiers using 836.5-MHz one-tone signal. The output power of one amplifier is 38.07 dBm with 10.61-dB power gain at the maximum PAE point which is 64.43%. The other amplifier is 37.88 dBm with 11.34 dB at 64.3%. The picture of fabricated PA and the test results of the two amplifiers are shown in Fig. 6.

To operate the amplifier at 44 V, double the drain bias voltage, the two amplifiers are stacked up through the virtual ground points and tested with same conditions except dc biases. The upper PA is biased with 44 V, and the drain bias point of the lower PA is connected to RF ground plane of the upper PA and the test results are shown in Fig. 7. The output power of the stacked-up PA is 40.62 dBm with the power gain of 11.56 dB at the maximum PAE of 58.8%. The slightly degraded performances may be related to the unbalance of the two amplifiers. However, we do not experience any problems to operate the amplifier at the twice higher supply voltage than the rated operation voltage of the transistors.

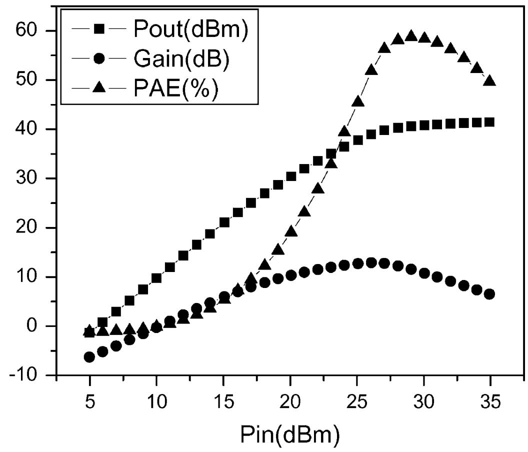


Fig. 7. High voltage operation test results of stacked push–pull amplifier.

IV. Conclusion

To operate a PA at a high supply voltage, two hybrid push–pull PAs are dc stacked-up through the virtual ground points of the balun and the RF outputs are series combined using the balun. In the new topology, all dc supply voltage is used for the power amplification with a low current, providing a high impedance level. The structure can operate at twice higher voltage than each amplifier can take and enhance the efficiency because of the low parasitic losses. The power performances of the high voltage operated amplifiers are similar to the each balanced amplifier. The supply voltage can be increased further by stacking the amplifier up more. The new circuit topology can be easily applied to the IC form and can be very useful for the CMOS PA with a low operation voltage.

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