

Figure 8 Frequency bandwidth measurement versus external magnetic field (H) for the YIG FRA

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THE FULLY-INTEGRATED CMOS RF POWER AMPLIFIER USING THE SEMILUMPED TRANSFORMER

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ABSTRACT: A semilumped output transformer for fully-integrated RF CMOS power amplifier is proposed in this paper. To demonstrate this transformer, a 2.5-GHz CMOS power amplifier is implemented with a 0.18- μm RF CMOS process used for WiMAX application. The power amplifier can achieve 39% PAE (power added efficiency) at 1 dB (1 dB compression point) and output power of 30 dBm. The linearity can satisfy the spectrum mask of the WiMAX signal requirement basically. © 2008 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 50: 2857–2860, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23811

Key words: CMOS; RF power amplifier; semilumped transformer; WiMAX

1. INTRODUCTION

The power amplifier in submicrometer CMOS processes tends to compete with the traditional SiGe and GaAs power amplifier in some advanced areas. Although there are still many challenges to exceed traditional designs, greater interests are being paid in the recent years. For mobile WiMAX 802.16e/m application, not only stringent linearity is required but also the high output power in the presence of an OFDM signal with a high 6 dB PAPR (peak-to-average power ratio) typically. With the second generation of WiMAX power amplifier being required, PAE at the average power regions is required above 20%. All this will result in consuming significant amounts of power. When all of these factors are combined, power amplifier design becomes very challenging; especially since overall power consumption is critical for handsets products [1]. The difficulty of CMOS power amplifier lies in the design, including the low breakdown voltage and poor harmonics. So far, the differential topology has been widely considered as the one of the best solution, and it features a virtual ground, which can cancel the even harmonics. Besides, it will reduce the disturbance to other blocks in the transceiver when it is fully integrated in the system [2]. Furthermore, the breakdown voltage is also increased by scale, and the output transformer will realize the high impedance transformation ratio and make the impedance matching more easily; in all, it will contribute to reduce the current and loss [3].

In this paper, we propose a fully-integrated CMOS power amplifier based on the semilumped output transformer with the $0.18\ \mu\text{m}$ CMOS process. The 30-dBm output power and 30-dB gain are implemented by using a three-stage network. The second harmonic is shortened at the drain of virtual ground of the output transformer and the source end to enhance the linearity. Therefore, the third intermodulation (IM3) is improved a lot at the average power region. To reduce the size of chip, some inductors used for interstage and output matching are replaced by the bonding wires.

2. SEMILUMPED OUTPUT TRANSFORMER DESIGN

To combine the high power at the output end, we have to design the proper transformer, which requires not only high impedance and voltage transformation ratio but also low loss [4, 5]. Although the distributed active transformer (DAT) overcame lots of disadvantages of the CMOS power amplifier and is very popular in the design, the coupling between the complex input and output feed lines is fatal to stability. For this reason, a semilumped transformer is proposed in this paper, which is originated from the traditional quarter-wave transformer. By adding the capacitance at the input and output end, we can reduce its size a lot. Using the theory of even and odd mode, we can decompose the transformer into the even and odd mode case, respectively, as shown in Figures 1(b) and 1(c), and it has been analyzed and verified successfully in the hybrid design [6]. The capacitance at the input and output will function differently; the capacitor C1 at the input will reduce the loss and the capacitor C2 at the output will affect the center frequency of transformer. By tuning the capacitances carefully, we can make the transformer resonant at the center frequency. The width of the transmission line is decided by the effect of metal migration and DRC (design rules check) of the process; the spacing of metals is tuned carefully to change the even and odd mode impedance of the transmission line and implement the maximal magnetic coupling. Process variation is also considered carefully in the design. All are evaluated and modified finely with

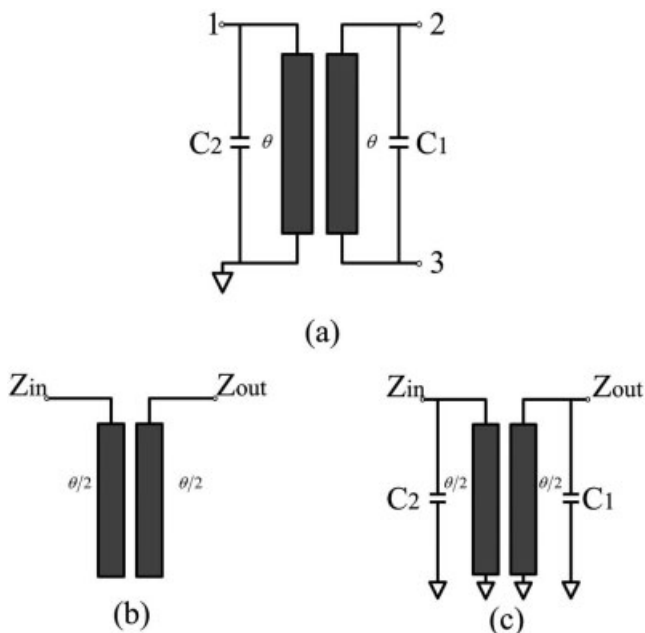


Figure 1 (a) The schematic of a semilumped transformer (b), the even mode of the semilumped transformer (c), and the odd mode of the semilumped transformer

the EM simulator-Sonnet v10.0. The loss of the transformer is about 0.8 dB at 2.5 GHz and the phase error is within 5 degrees and the bandwidth is about 300 MHz within 1 dB loss. The size of transformer is $700 \times 280\ \mu\text{m}^2$, which is one of the most compact transformers reported and the capacitance C1 and C2 are 7.55 pF and 2.22 pF with the EM simulator results, respectively.

3. POWER AMPLIFIER DESIGN

A 2.5-GHz power amplifier combined with the semilumped transformer is designed in this paper. To improve the gain, we employ the three stages so as to offer 30-dB gain and only the capacitor is employed to isolate DC bias and interstage matching. The schematic and chip layout are demonstrated in Figure 2, and all components are fully-integrated including the input balun. The gate length is selected with the thick oxide model with $0.35\ \mu\text{m}$ for higher breakdown voltage. The total gate width of the power cell is $2 \times 3360\ \mu\text{m}$ and the scale of the second driver stage and first driver stage are $2 \times 960\ \mu\text{m}$ and $2 \times 192\ \mu\text{m}$, respectively, which are reduced by three fourths of the size when compared with the former stage, the total chip area is $1.8 \times 1.2\ \text{mm}^2$, including all the test pads. The gate bias of the power stage is at the deep class AB to reduce the DC current consumption and improve the PAE; and the gate biases of the first and second driver stage are at light class AB to offer higher gain. A-3.3 V supply voltage (V_{dd}) is fed into the drains of the three stages through the bonding wires, and some RF short capacitors are parallelly attached on the test PCB to contribute to the stability. By adding the matching capacitors at the input and output, both are matched to $50\ \Omega$. The virtual ground at the center of transformer has two functions, one is to offer the DC bias for the drain at the power stage, and the other one is to shorten the second harmonic with the on-chip capacitance and serial bonding wire. Actually, the quality factor of the second harmonic will be reduced because of the resistance introduced by the transformer, but it will decrease the number of pads at the middle of layout (which can reduce the coupling with other bonding wires).

The losses of the on-chip and off-chip components are included in the power amplifier design. Figure 3 shows the gain and PAE versus the output power. The power at P1dB can achieve 30 dBm and PAE is 39% at P1dB and is about 23% at the 5dB back-off region.

Figure 4 shows the output spectrum under the WiMAX signal test with 10-MHz bandwidth. The WiMAX spectrum mask require the frequency offset point at -4.75MHz , $-5.25\ \text{MHz}$, $-9.75\ \text{MHz}$, and $-14.75\ \text{MHz}$ to be lower than 0 dBr, $-25\ \text{dBr}$, $-32\ \text{dBr}$, and $-50\ \text{dBr}$, respectively (dBr is dB relative to the maximum spectral density of the signal). It is covered basically by the mobile WiMAX spectrum mask over the full range of output power.

4. CONCLUSION

A semilumped output transformer combined with the fully-integrated RF CMOS power amplifier is proposed in this work with a $0.18\text{-}\mu\text{m}$ RF CMOS process. The power amplifier achieved a PAE of 39% at a maximum output power of 30 dBm and over 20% at the 5 dB backoff region, and the linearity can satisfy the spectrum mask of the mobile WiMAX signal basically, which can work at 2.5 GHz properly.

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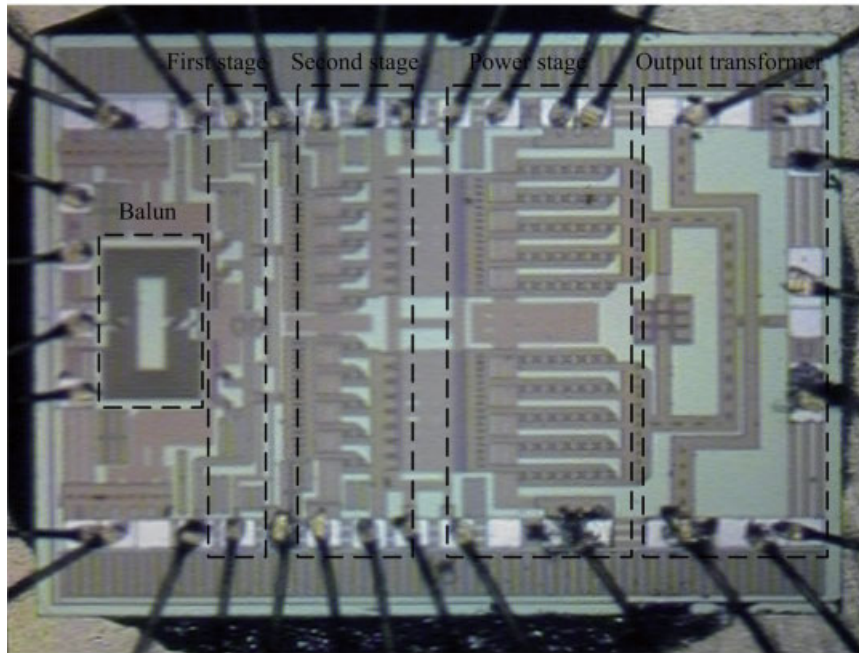
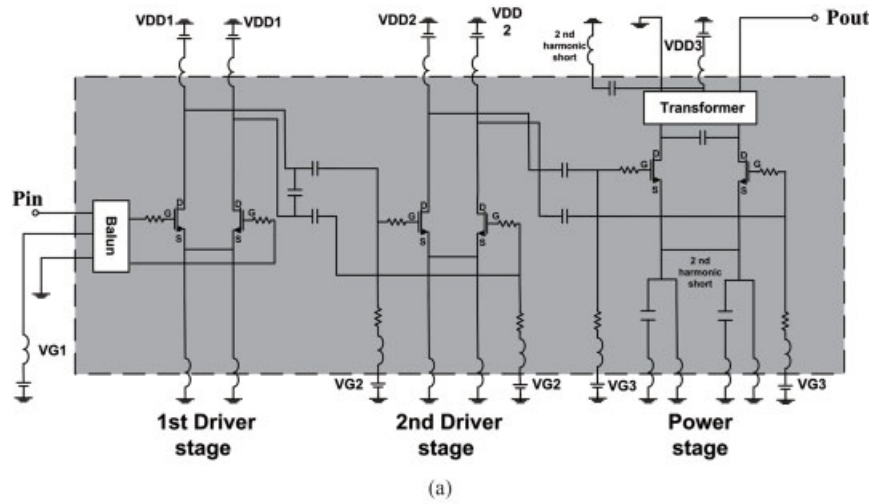


Figure 2 (a) The schematic of the power amplifier and (b) the chip layout. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

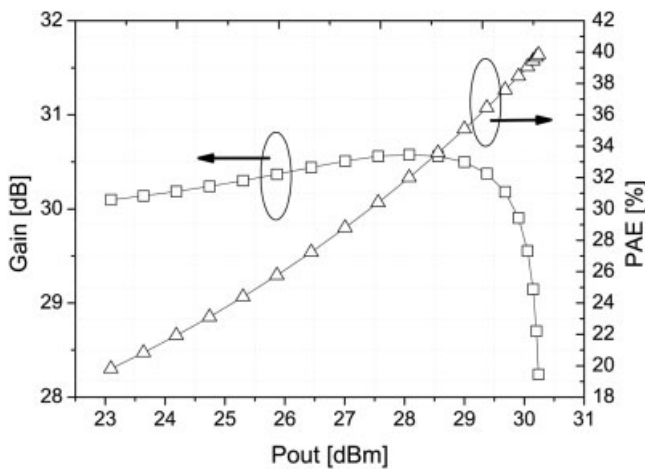


Figure 3 Gain and PAE versus output power

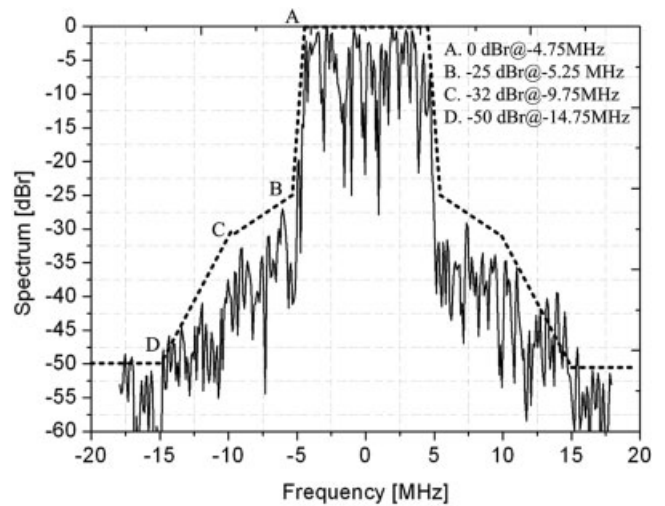


Figure 4 Spectrum for the WiMAX signal with 10-MHz bandwidth

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A SPIRAL-SHAPED MONOPOLE ANTENNA FOR QUAD-BAND OPERATION OF MOBILE HANDSETS

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ABSTRACT: This article presents the design and fabrication of a quad-band spiral-shaped monopole antenna for application in a GPS (1575 \pm 10 MHz)/DCS (1710–1880 MHz)/PCS (1850–1990 MHz) with a UMTS (1920–2170 MHz) band. To obtain sufficient bandwidth in $V_{\text{SWR}} < 2$, an air layer is inserted between the ground plane and the substrate. A spiral-shaped monopole antenna that has a quad-band characteristic is used. Important design parameters are the spiral radiator gap's width and length, the air-gap's height, and the feed point's position. From these optimized parameters, a spiral-shaped monopole antenna is fabricated and measured. The measured results of the fabricated antenna are obtained from all bands at 940 MHz bandwidths in $V_{\text{SWR}} < 2$ referenced to the center frequency, and the individual gain at 2.2 dBi, 2.5 dBi, 2.6 dBi, and 2.6 dBi. The experimental 3 dB beam width is shown to be broad across the pass band in the E-plane, and 74°, 68°, 64°, and 60°, respectively. © 2008 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 50: 2860–2863, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23810

Key words: spiral-shaped antenna; Quad-band; GPS; PCS; DCS; UMTS

1. INTRODUCTION

Wireless communications have been developed widely and rapidly in the modern world, which leads to a great demand for designing compact, low-profile, and multi-band antennas. To meet these requirements, compact high-performance multi-band planar antennas with good radiation characteristics have been designed for wireless applications [1–9]. Many antenna structures have been

proposed for this application, such as a compact helical antenna using the normal-mode of two helix wires [4], a disk-loaded monopole antenna using parallel strip line elements [5] and a planar inverted F antenna with various feeding structures [6]. Although these antennas have good antenna characteristics, however, their large size makes them difficult for use as internal antennas.

It is well-known that the resonance frequency of an antenna for a given size can be effectively reduced by maximizing the current path on the conductor in the antenna. A spiral-shaped conductor is a good candidate to obtain such characteristics [7]. In addition, it has been shown that the bandwidth of an antenna can be improved by using mutual coupling between two radiators located in very close proximity [8]. Spiral antennas have been the subject of research for several decades. Since their introduction in the 1960's, together with various other microstrip patch antennas, spiral antennas have emerged as leading candidates for applications requiring circularly polarized broadband antennas [10].

Various shapes and types of spiral antennas have been designed and fabricated. Spirals can have a single arm or multiple arms, and have been realized in a microstrip form [11, 12] as well as in slot forms [13, 14]. However, spiral antennas have shortcomings as well. They require deeper lossy cavities and special attention to a nonplanar balun/impedance transformer network design, which renders the antenna structure as thick and complicated. Recently, several designs of planar spiral antennas that do away with complex feeding networks were proposed [15–18]. These antennas are planar and easy to fabricate, and they do not need a matching network. Several new designs of spiral antennas therefore fall under the modified type, as opposed to the conventional type [19, 20].

In this article, we present an experimental study using a technique similar to that used for a spiral-shaped monopole antenna. A modified spiral-shaped monopole antenna, with a proposed quad-band operation based on modified spiral radiator gap's techniques. This behavior makes the operating bandwidths of the antenna's bands larger than 43% (2:1 VSWR), allowing the antenna to cover GPS/DCS/PCS and UMTS bands for quad-band operation. In addition, the proposed quad-band monopole antenna occupies a small area measuring only $10 \times 30 \times 5 \text{ mm}^3$ inside the mobile phone. The results of the experiment that was conducted on the antenna's broadband impedance bandwidth, radiation pattern, and gain are discussed in detail below.

2. ANTENNA DESIGN

Figure 1 shows the geometry of the spiral-shaped monopole antenna. This antenna has been designed only for the spiral-shape of smaller antenna sizes. The proposed antenna is based on a modified spiral radiator gap's techniques. The modified spiral-shape enables quad-band operation. The radiating element occupies a $10 \times 30 \text{ mm}^2$ area and uses air-layer (5 mm thick) substrate with a permittivity of one. A $40 \times 60 \text{ mm}^2$ ground plane was used in this study. An air-filled substrate was applied to help to efficiently increase the desirable impedance bandwidth. The radiating element and the ground plane form a 5 mm thick air-layer substrate. The radiator width and length, the air-layer's thickness, and the feeding point's position have been varied in steps, with the bandwidth calculated at each step until the maximum bandwidth has been obtained and optimized for broadband use.

After a thorough parametric study of the modified spiral-shaped monopole antenna, the proposed antenna's optimum design parameters were set as follows: $L = 30 \text{ mm}$, $L_1 = 8 \text{ mm}$, $L_2 = 11 \text{ mm}$, $L_3 = 15 \text{ mm}$, $W = 10 \text{ mm}$, $W_1 = 1 \text{ mm}$, $W_2 = 8 \text{ mm}$, $G_L =$