

A Parallel Power Amplifier With a Novel Mode Switching Control

Kichon Han and Bumman Kim, *Fellow, IEEE*

Abstract—Two parallel operating power amplifiers (PAs) are controlled by a novel mode switch for high efficiencies at both the back-off power region and high power region. The mode switch is realized by the base-collector (BC) junction diode which reuses the dc current of the low power mode amplifier. A 836 MHz CDMA PA has been demonstrated using InGaP/GaAs heterojunction bipolar transistor with fully integrated matching component for small package and low cost. It shows a 13 mA idle current, 15.4% power added efficiency (PAE), -48 dBc ACPR1 at 16 dBm of the low power mode operation and a 40.5% PAE, -46 dBc ACPR1 at 28 dBm of the high power mode operation.

Index Terms—Back-off power operation, mode switching, power amplifier (PA), power-added efficiency (PAE).

I. INTRODUCTION

As mobile handsets are required to perform multiple functions (such as camera, DMB, MP3P) and be slimmed for convenience, power saving is the main issue for the handset designers. Since the Power amplifier (PA) is the main current consuming component in the handsets, there are several reports to increase power-added efficiency (PAE) at back-off output power level [1]–[6].

The dynamic power-supply voltage control [1] and the Doherty load modulation technique with dynamic bias control [2] seem to be the most effective approaches for the overall efficiency enhancement, but they have complicated circuit structures with high cost. The dynamic quiescent bias current control [3], which uses the feedback power level information to reduce the idle current, can save power without increasing the size and cost. But the efficiency enhancement is limited to the power level under 10 dBm because of the current increase of the class AB bias operation characteristic. The parallel power amplification with the path control by a switch is a very simple solution for the problem with low cost [5], [6]. Although conventional PAs can be used for the low and high power modes, it is not easy to match the two PAs simultaneously. And it requires low/high power mode calibration and additional programming to set the mode switching point with hysteresis for stable operation. Also, the handset designers concern is primarily the PAE and linearity at

the high power, and it requires a careful design to enhance the low power mode PAE without degrading that of the high power mode.

In this letter, we report a novel mode switching method for the parallel power amplification to enhance the low power mode PAE without affecting the high power mode PAE. At first, the operating principle is discussed. Then, the PA is realized for 836 MHz cellular CDMA band application by InGaP/GaAs heterojunction bipolar transistor (HBT) process and the measured results are shown.

II. PRINCIPLE OF OPERATION

Fig. 1(a) shows the simplified schematic of the proposed PA. It is similar to the conventional PA except the added parallel power stage, which is optimized for the PAE at the low output power. The series switch SW1 is used in the low power path to prevent the turn-on of the low power amplifier (LPA) at the high power mode operation. The switch is not required in the high power path since a relatively low power is applied into the path when it is off. The bias circuits are composed of a simple combinational logic and current control element.

The Base/Collector junction diode (D1), which is located at the low power mode path, turns on by the collector current of the low power mode amplifier. When the diode is turned on, its equivalent circuit becomes a small resistor whose value changes according to the size and the turn-on current. The resistance decreases as the output power increases. Fig. 1(b) shows the low power mode equivalent circuit. The series inductor L_1 with the parallel capacitor C_1 transforms R_O to the optimum low mode impedance R_{LM} . If $R_{LM} = m \cdot R_O$ and $R_{ON} = (n \cdot V_T / I_D) \ll R_O$, (1) and (2) give the low pass matching component values of C_1 and L_1

$$C_1 = \frac{\sqrt{m-1}}{\omega_0 \cdot m \cdot R_O} \quad (1)$$

$$L_1 = \frac{R_O \cdot \sqrt{m-1}}{\omega_0} \quad (2)$$

Fig. 1(c) shows the high power mode equivalent circuit. When the diode turns off, the equivalent circuit is a small capacitor (C_{OFF}) and the value changes also with the size and bias condition. The series diode connection with the matching components reduces the equivalent off-state capacitive value and makes the resonance frequency away from the operating frequency. If $C_{OFF} = C_1/k$ and $C_{LPA} \ll C_1$, (3) and (4) give the equivalent capacitance and the resonance notch frequency

$$C_{EQ} = \frac{C_{OFF} \cdot (C_{LPA} + C_1)}{C_{OFF} + (C_{LPA} + C_1)} = \frac{C_1}{k+1} \quad (3)$$

$$\omega_{res} = \frac{\omega_0 \cdot \sqrt{m \cdot (k+1)}}{\sqrt{m-1}} \quad (4)$$

where C_{LPA} is the output capacitance of off-state LPA.

Manuscript received September 9, 2007; revised November 2, 2007. This work was supported in part by the Korean Ministry of Education under the BK21 Project and by the Center for Broadband OFDM Mobile Access (BrOMA) at POSTECH through the ITRC Program of the Korean MIC, supervised by IITA. (IITA-2007-C1090-0701-0037).

The authors are with the Department of Electrical Engineering, Pohang University of Science and Technology, Gyeongbuk 790-784, Korea (e-mail: moonight@postech.ac.kr).

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LMWC.2008.916813

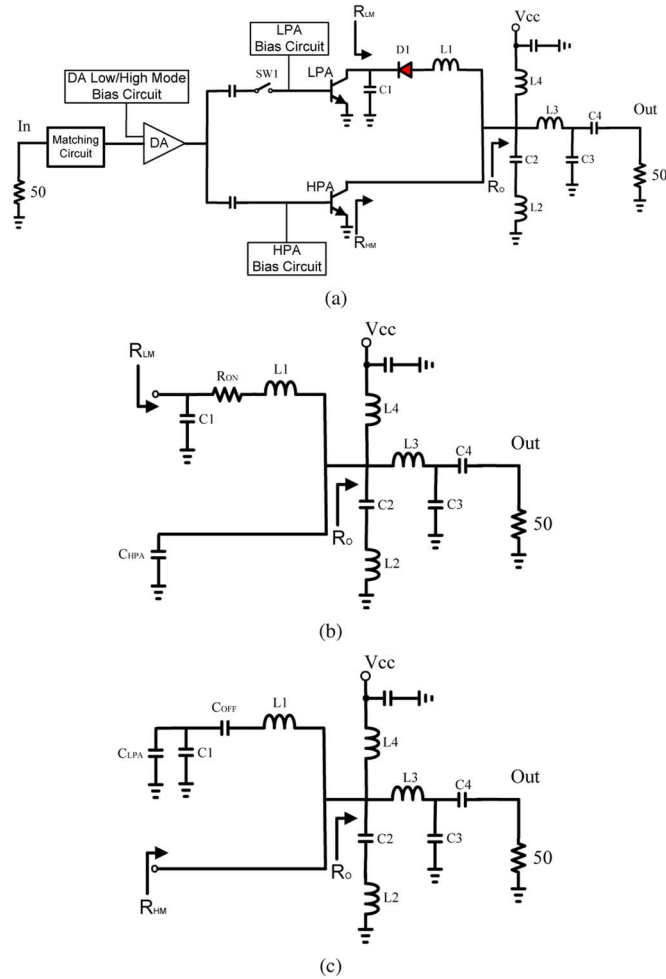


Fig. 1. (a) Schematic of the PA with an output load switching diode. (b) Equivalent output circuit for the low power mode operation. (c) Equivalent output circuit for the high power mode operation.

The resonance notch frequency is $\sqrt{k+1}$ times higher than the one which is close to the in-band frequency. If C_{OFF} is small enough, the parallel connection of the low mode matching components L1, C1, C_{OFF} do not affect to the high power mode operation.

III. EXPERIMENTAL RESULTS

The proposed PA is fabricated using InGaP/GaAs HBT process. We use an 360 μm emitter area HBT as an unit-cell. The DA and LPA use 2 unit-cells and the HPA uses 16 unit-cells. For the switch diode, 8 unit-cells are used. All the output matching capacitors are integrated on chip to reduce cost and the output matching inductances are realized using bonding wires. Measurements are performed on a 400 μm thick 2 layer FR4 printed circuit board and a chip-on-board assembly is exploited.

Fig. 2 shows RF power and linearity performances of the amplifier for reverse-link IS-95A signal with chip rate of 1.2288 Mcps at 836 MHz CDMA band. Because of low probability of transmission above 16 dBm [5], systems usually set this power level as a switching point. So we have measured up to 18 dBm for the low power mode and 29 dBm for the high power mode. Although there are diode turn-on loss at the low

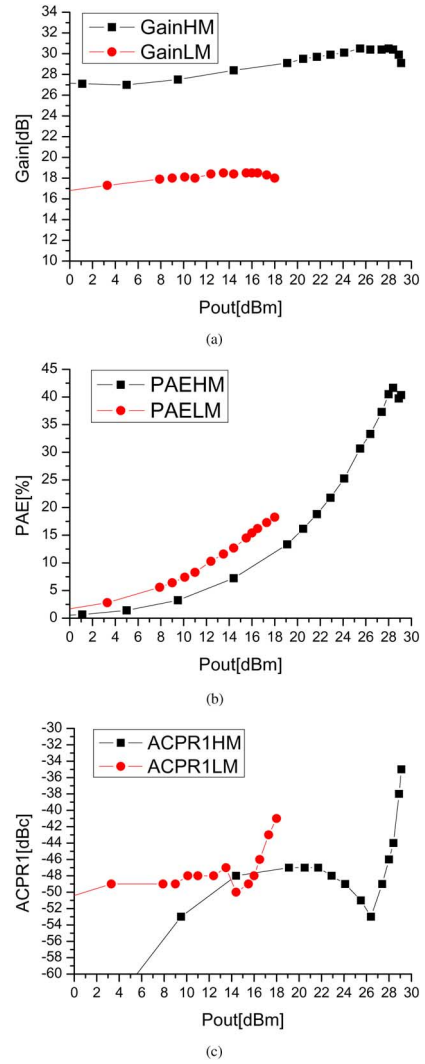


Fig. 2. Performances of the proposed PA. (a) Gain. (b) PAE. (c) ACPR1.

power mode and parallel parasitic loading at the high power mode, the measured results show good performances, indicating that it is a good candidate for the high PAE amplifier. For the low mode operation, the total quiescent current is 13 mA with $V_{CC} = 3.4$ V. The PAE is 15.4% at Pout of 16 dBm, and the ACPR are -48 dBc and -56 dBc at 885 KHz and 1.98 MHz offsets, respectively. For the high mode operation, the total quiescent is 56 mA with $V_{CC} = 3.4$ V. The PAE is 40.5% at Pout of 28 dBm, and the ACPR are -46 dBc and -54 dBc at 885 KHz and 1.98 MHz offsets, respectively.

Fig. 3 shows a micrograph of MMIC chip whose size is 1.0×1.2 mm².

IV. CONCLUSION

A novel diode switching method for parallel PA is proposed to reduce PA current consumption at the back-off power region, without any increased loss at the high power region. We have derived a simple equation for the diode size and have demonstrated it using InGaP/GaAs HBT process. For a small size package and low cost, all matching capacitors are integrated on-chip and inductors are implemented using bonding wires. The PA provides 15.4% PAE with ACPR1 less than -48 dBc at an output power

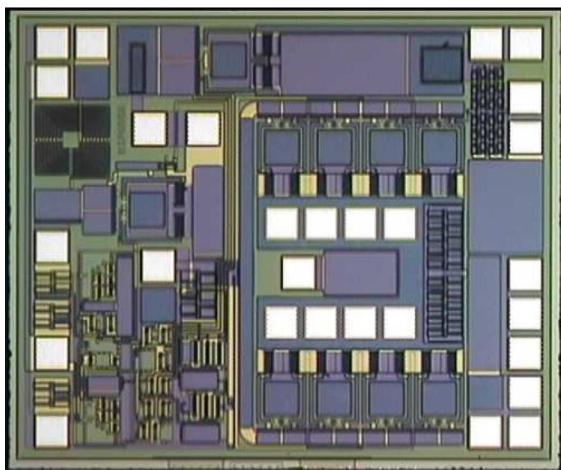


Fig. 3. Micrograph of MMIC chip.

level of 16 dBm and 40.5% PAE with ACPR1 less than -46 dBc at 28 dBm.

REFERENCES

- [1] G. Hanington, P. F. Chen, P. M. Asbeck, and L. E. Larson, "High-efficiency over amplifier using dynamic power supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.
- [2] J. Nam and B. Kim, "The Doherty power amplifier with on-chip dynamic bias control circuit for handset application," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 4, pp. 633–642, Apr. 2007.
- [3] Y. W. Kim, K. C. Han, S. Y. Hong, and J. H. Shin, "A 45% PAE/18 mA quiescent current CDMA PAM with a dynamic bias control circuit [power amplifier module]," in *IEEE RFIC Symp. Dig.*, Jun. 2004, pp. 365–368.
- [4] S. Kim, K. Lee, P. J. Zampardi, and B. Kim, "CDMA handset power amplifier with diode load modulator," in *IEEE MTT-S Int. Dig.*, Jun. 2005, pp. 653–656.
- [5] J. H. Kim, J. H. Kim, Y. S. Noh, and C. S. Park, "An InGaP-GaAs HBT MMIC smart power amplifier for W-CDMA mobile handsets," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 905–910, Jun. 2003.
- [6] G. Hau, S. Caron, J. Turpel, and B. MacDonald, "A 20 mA quiescent current 40% PAE WCDMA HBT power amplifier module with reduced current consumption under backoff power operation," in *IEEE RFIC Symp. Dig.*, Jun. 2005, pp. 243–246.