

A New RF CMOS Gilbert Mixer With Improved Noise Figure and Linearity

Jehyung Yoon, *Student Member, IEEE*, Huijung Kim, Changjoon Park, *Student Member, IEEE*, Jinho Yang, Hyejeong Song, Sekyeong Lee, and Bumman Kim, *Fellow, IEEE*

Abstract—The noise figure of an RF CMOS mixer is strongly affected by flicker noise. The noise figure can be improved using pMOS switch circuits, which insert current at the on/off crossing instants of the local oscillator switch stage because the circuits reduce the flicker noise injection. When it is applied to a conventional Gilbert mixer, the injection efficiency and linearity are degraded by the nonlinear parasitic capacitances of the pMOS switch circuits and the leakage through the parasitic path. We propose the pMOS switch circuits with an inductor, which tunes out the parasitic components at $2f_o$ and closes out the leakage path. The mixer fabricated in 0.13- μm CMOS at 2.4-GHz center frequency has provided improved characteristics for linearity and noise figure.

Index Terms—CMOS, direct conversion, double-balanced mixer, flicker noise, Gilbert mixer, IF, $1/f$ noise.

I. INTRODUCTION

BY VIRTUE of rapid development of wireless communication technology, many types of mobile communication devices, such as cellular phones, global-positioning systems, and wireless broadband Internet, have been introduced in our daily life. For the system, it is highly desirable to develop low-power system integrated circuits (ICs), which integrate the various functions on a single chip. The CMOS process, which lowers production cost and allows high-level integration, is widely used for the applications. Among receivers for the mobile communication systems, a direct conversion receiver (DCR) is a valuable solution for low-cost and low-power implementation. However, it is still difficult to design the DCR with the CMOS due to comparatively inferior properties such

Manuscript received August 2, 2007; revised November 12, 2007. This work was supported by the Korean Government (MOST) under Korea Science and Engineering Foundation (KOSEF) Grant R01-2007-000-20377-0, by the Ministry of Commerce, Industry and Energy (MCIE), Korea, under the Development of Transceiver System for Next Generation Wireless Communication Project supervised by the Next Generation New Technology Business, and by the Ministry of Information and Communication (MIC), Korea, under Information Technology Research Center (ITRC) Support Program IITA-2007-C1090-0701-0037 supervised by the Institute of Information Technology Advancement (IITA).

J. Yoon, C. Park, H. Song, S. Lee, and B. Kim are with the Department of Electrical Engineering, Pohang University of Science and Technology, Gyeongbuk 790-784, Korea (e-mail: yjh7605@postech.ac.kr; bmkim@postech.ac.kr).

H. Kim is with the RF Team, System Large Scale Integration (LSI) Division, Semiconductor Business, Samsung Electronics Company Ltd., Gyeonggi-Do 431-836, Korea.

J. Yang is with SK Telecom, Seoul 100-999, Korea.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TMTT.2008.916942

as poor noise performance, low breakdown voltage, and small gain; the critical problem is the poor noise performance [1].

In the DCR, a double-balanced Gilbert mixer is the most popular one due to low RF and local oscillator (LO) feed-through [2], [3]. However, high noise figure of the mixer degrades the entire receiver performance [4]. In the LO stage of the mixer, switch operation for the mixing has on/off transition, and during the transition, a high flicker noise is delivered to the output [5]–[7]. It is proposed to use pMOS switch circuits to reduce the noise injection [8]. The pMOS inserts current into the mixer core at the on/off instant, and the on/off of the LO switch stage is sharpened. A large pMOS can deliver more current and make a sharper turn on/off of the stage than a small one. As size of the pMOS becomes large, comparable to the core cell, the nonlinear capacitances of the pMOS produce harmonics and form leakage paths for the insertion current. Therefore, the capacitance effects should be minimized to operate the mixer properly. In order to reduce the effects, we have proposed to tune out the capacitances at $2f_o$ using a parallel inductor. The tuned circuit eliminates the leakage path for the current, which mainly has a $2f_o$ component, and reduces harmonic generation from the nonlinear capacitances due to the inductive padding effect.

In order to demonstrate the improved performance, we have designed three types of mixers, which are: 1) a conventional Gilbert mixer; 2) a mixer with pMOS switch circuits; and 3) the proposed mixer. The mixers are compared for the noise figure and linearity. In this paper, we describe the linearity and noise performance of each type of mixer in Section II. In Sections III and IV, we describe the measured results and give conclusions.

II. IMPROVEMENT OF THE NOISE FIGURE AND THE LINEARITY OF A GILBERT MIXER

A. Noise Figure Improvement Using pMOS Switch Circuits

A double-balanced Gilbert mixer, shown in Fig. 1, comprises a transconductance stage, an LO switch stage, and an output load stage. The RF input signal is amplified in the transconductance stage, down-converted to an IF current signal in the LO switch stage, and then converted to a voltage signal by the output load stage. The dominant noise source of the DCR mixer is flicker noise of the LO switch stage because the IF signal is located at close to dc frequency, which is below the corner frequency of the noise. The noise influence on the LO switch core is described by two mechanisms [5]. One is the direct influence that the $1/f$ noise of the stage is sampled at $2f_o$ during the on/off transit time aperture. The other one is the indirect influence of charging and discharging of the parasitic capacitance (C_p) of the stage by the flicker noise at $2f_o$. Concerning the direct flicker

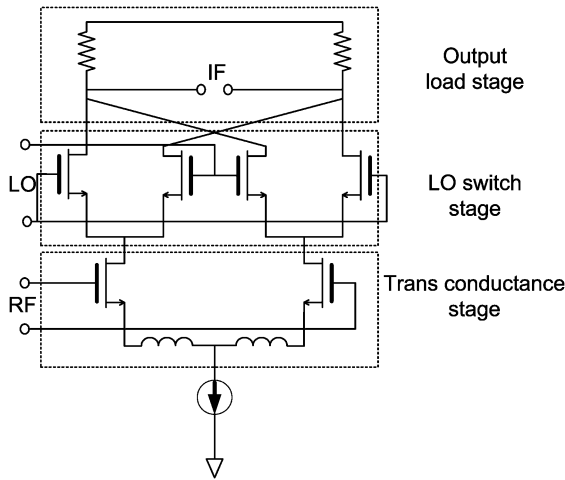


Fig. 1. Conventional double-balanced Gilbert mixer in DCR.

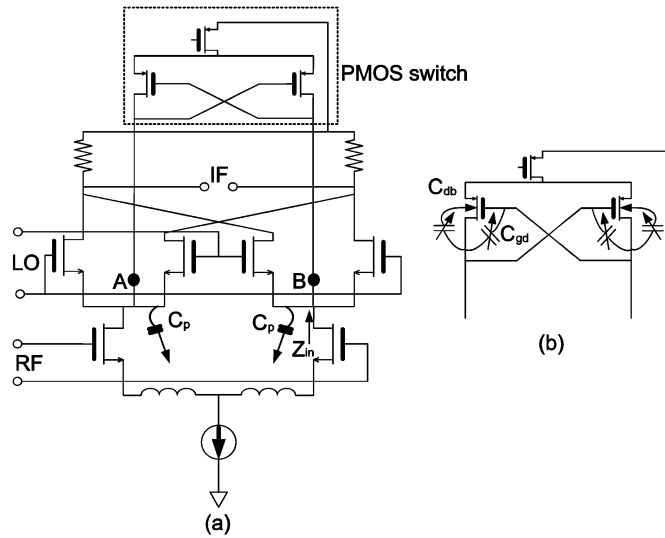


Fig. 2. (a) Gilbert mixer with pMOS switch circuits. (b) pMOS switch circuits with parasitic capacitances.

noise influence, the noise sampling aperture is determined by the switching transit time of the LO stage and the noise can be reduced by narrowing the aperture. The aperture can be reduced by using the pMOS switch circuits in the conventional mixers, as shown in Fig. 2(a) [8]. The pMOS switch circuits provide current at nodes A and B during every switching instant. As the current flows into the switch stage, the sampling aperture is reduced and the noise figure of the mixer is improved. For an effective insertion of the current, the pMOS cell size should be large enough to generate a proper amount of current. However, the increased pMOS has large parasitic capacitances such as the drain–gate capacitance (C_{gd}) and drain–body capacitance (C_{db}), as shown in Fig. 2(b). The capacitances, together with C_p , provide leakage paths for the insertion current and limit the amount of the current. Moreover, the capacitances are nonlinear, generating harmonics.

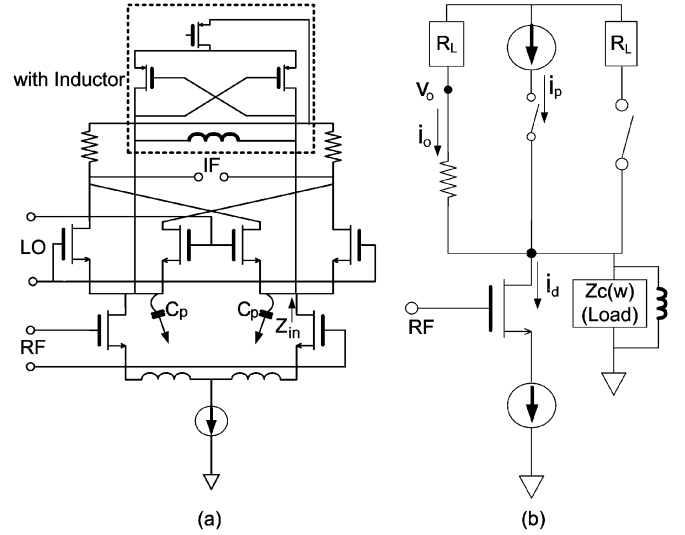


Fig. 3. (a) Proposed Gilbert mixer with pMOS switch circuits resonated by an inductor. (b) Equivalent circuits of the single-stage mixers.

B. Noise Figure and Linearity Improvements of a Gilbert Mixer With Inductive Tuned pMOS Switch Circuits

To improve the noise figure further by a proper operation of the pMOS switch circuits, an efficient current insertion method should be found. For this purpose, we have employed a parallel inductor to tune out the capacitances at $2f_o$, as shown in Fig. 3(a). The equivalent circuit is shown in Fig. 3(b). The nonlinear impedance (Z_C) comprises the nonlinear capacitances, such as the C_{gb} and C_{db} , negative transconductance ($-g_{m,p}$) of the pMOS switch circuits, and parasitic capacitance (C_p). The insertion current (i_p) mainly has a $2f_o$ component, and the current cannot leak through the parallel resonated circuit. Therefore, the insertion current can be delivered very efficiently, reducing the direct flicker noise contribution. The flicker noise of the switch core is indirectly transmitted by charging and discharging of C_p [5], [14] and the reduction of the C_p effect by the resonant circuit also suppresses the indirect noise. Table I shows spectral density of the flicker noise in the switch core for each type of mixer. The flicker noise contribution of the conventional Gilbert mixer is reduced by the pMOS switch circuits. The proposed circuit shows a significant further improvement of the flicker noise effect.

We have found that the resonant circuit can enhance the linearity due to the inductive padding effect for the nonlinear capacitances. Harmonics of conventional Gilbert mixers are generated mainly by nonlinearity of the transconductance stage [9]. Since the LO switch stage operates as an on/off switch and the output load stage is a passive component, neither of them generates any significant distortions. In the transconductance stage, the harmonics are generated mainly from g_m (transconductance), g_{ds} (output conductance), and C_{gs} (gate–source capacitance); the dominant influence is from g_m nonlinearity [10], [11]. The nonlinear g_m can be expressed by a Taylor series expansion as follows [12], [13]:

$$g_m = g_{m1} + g_{m2}v_{gs}^1 + g_{m3}v_{gs}^2 + \dots \quad (1)$$

TABLE I
FLICKER NOISE CONTRIBUTION FROM LO SWITCH CELL

	Flicker noise of LO switch cell [V^2/Hz]	Total noise spectral density [V^2/Hz]
Conventional Gilbert mixer	1.47e-15	1.5e-15
with PMOS switch circuits	4.8e-16	5.4e-16
with PMOS switch circuits tuned by inductor	1.27e-16	1.69e-16

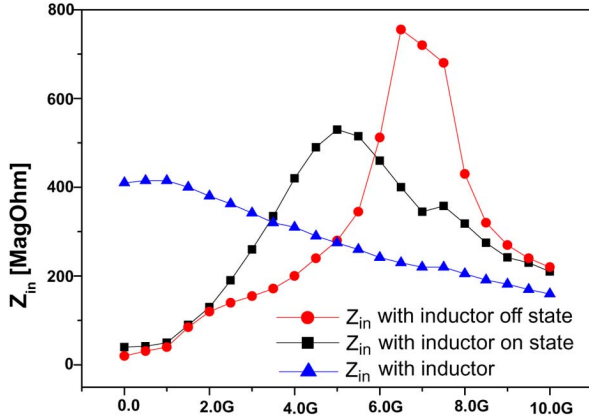


Fig. 4. Input impedance results seen at the source of the switch cell.

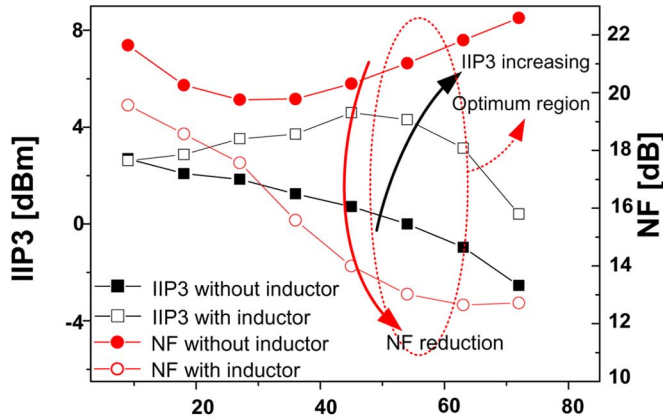


Fig. 5. pMOS size-dependent characteristics.

Corresponding drain current of the transconductance is described as a function of g_m (transconductance) and gate-source voltage (v_{gs})

$$i_d(t) = g_{m1}v_{gs}(t) + g_{m2}v_{gs}^2(t) + g_{m3}v_{gs}^3(t) + \dots \quad (2)$$

However, the pMOS switch circuits provide additional large nonlinearity components such as C_p , C_{gb} , and C_{db} , as shown in Fig. 2(b). Due to the nonlinear elements of the pMOS switch circuits, linearity of the mixer is degraded. For the resonant circuit, the nonlinear capacitances are padded by the inductor and the harmonics generated are reduced significantly. Z_C consists of C_p , C_{gb} , and C_{db} and is represented by C_C . The admittance Y_{in} of $Z_C \parallel j\omega L$ at ω_{RF} , which is the operating frequency, is given by

$$Y_{in}(w) = jw_{RF}C_C + \frac{1}{jw_{RF}L} = \frac{1}{jw_{RF}L} (1 - w_{RF}^2 C_C L). \quad (3)$$

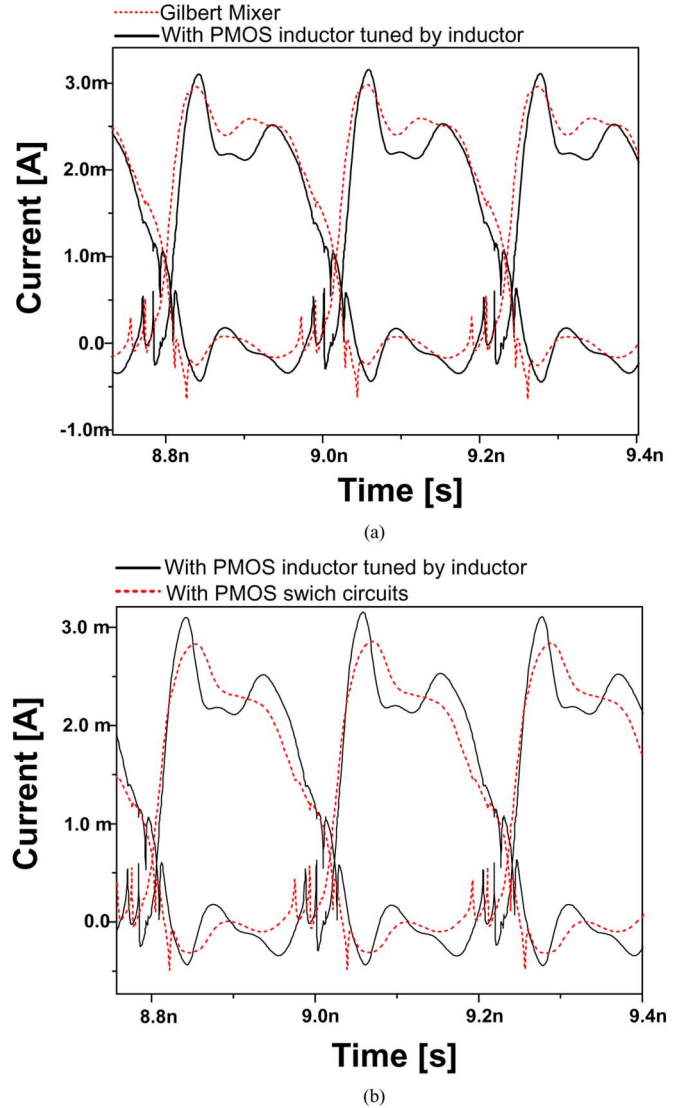


Fig. 6. Comparison for drain currents of LO switch cell: (a) with Gilbert mixer and with pMOS switch circuit tuned by inductor and (b) with pMOS switch circuit tuned by inductor and with pMOS switch circuit.

For a variation of the C_C by $\pm\Delta C_C$, due to the switching action, the Y_{in} variation is given by

$$Y_{in}(w) = \frac{1}{jw_{RF}L} (1 - w_{RF}^2 (C_C \pm \Delta C_C) L). \quad (4)$$

Equation (4) can be further simplified to

$$Y_{in}(w) = jw_{RF}3C_C \left(1 \mp \frac{\Delta C_C}{3C_C}\right) \quad (5)$$

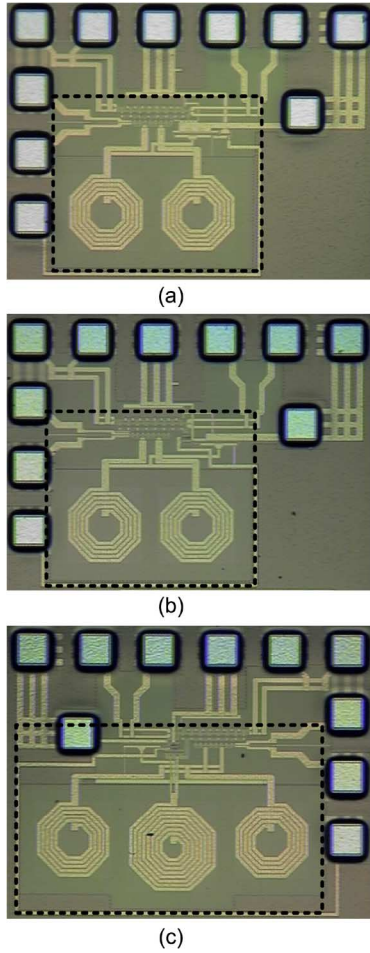


Fig. 7. Photograph of: (a) conventional Gilbert mixer, (b) with pMOS switch circuits, and (c) with pMOS switch circuits and inductor.

where $2\omega_{RF} = 1/\sqrt{LC_C}$. Equation (5) shows that effective variation of C_C is reduced by a factor of 3, reducing the non-linearity. Fig. 4 shows the calculated impedances of Z_{in} for the on and off states of the pMOS switch. It clearly shows the resonance at $2f_o$ for the on stage. The impedances of the circuits at f_o is similar for the on and off stages, behaving quite similarly.

C. PMOS Size Optimization

For the circuit design, size of the pMOS is very important and should be optimized. For this purpose, we have simulated the noise and linearity performances as a function of the gatewidth. The noise figure of the mixer is simulated using Cadence Spectre-RF, which can compute the down-converted noise behavior. We have calculated for the case with and without the inductor and the results are summarized in Fig. 5. Our simulation shows that when the inductor is not employed, the noise figure of the mixer is improved as the width is increased. However, for a large width PMOS, more than $40 \mu\text{m}$ in our case, the noise figure is degraded rather than improved due to the current leakage through the capacitances. When the inductor is employed, the noise figure is improved continuously by a large amount up to the gatewidth of $60 \mu\text{m}$, mainly due to the proper current insertion.

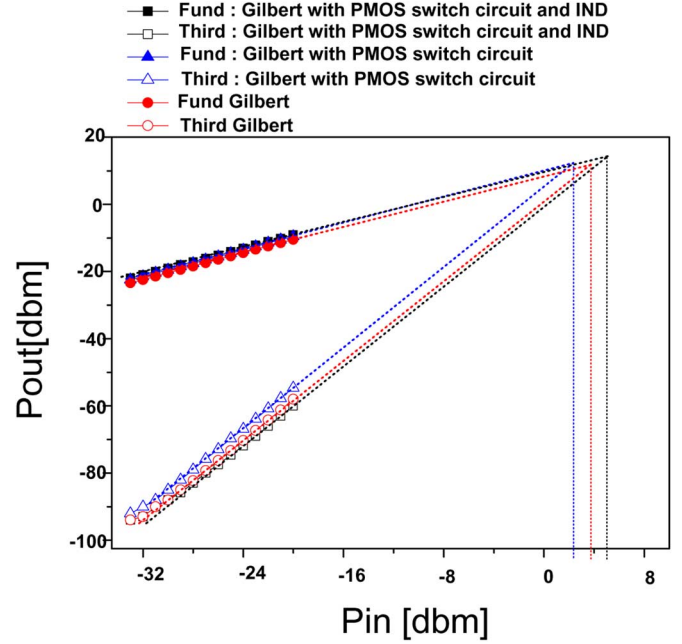


Fig. 8. Measured results of the fundamental and third harmonic powers.

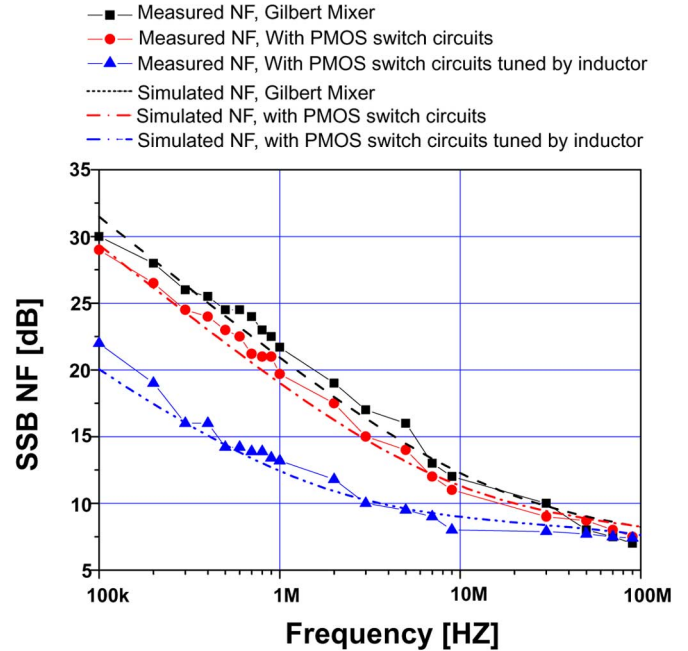


Fig. 9. Measured and simulated SSB noise figure.

As shown in Fig. 5, the pMOS switch circuit degrades linearity of the mixer, and the large pMOS mixer has a low third-order input intermodulation (IIP3), as expected. When the non-linear capacitances are tuned out by the inductor, the mixer linearity is significantly improved, but the gatewidth increases further, large current flows through the nonlinear capacitances, and the IIP3 is degraded. For the pMOS gatewidth of up to $50 \mu\text{m}$, the nonlinearity of the pMOS is not a significant factor in our case. From Fig. 5, we can conclude that the optimum size of the pMOS with the tuned inductor is around $50\text{--}60 \mu\text{m}$. Fig. 6 show waveforms of the drain current of the LO switch stage.

TABLE II
PERFORMANCE OF THE THREE MIXERS

	Conventional Gilbert Mixer	with PMOS switch circuits	with PMOS switch circuits tuned by inductor
Conversion gain (dB)	10.1	11	11.4
IIP3 (dbm)	3.8	2.7	4.4
SSB NF (dB) @ 1MHz	21.7	19.7	13.2
Tail current (mA)	6	6	6
Core chip area without pads(mm ²)	0.53 × 0.6	0.53 × 0.6	0.56 × 0.87

Samsung 0.13 μ m RF CMOS

They clearly show that the waveforms are sharpen by the effective current insertion.

III. REALIZATION AND MEASURED RESULTS

We have designed the three types of mixers, which are: 1) a conventional mixer; 2) a mixer with the pMOS switch circuit; and 3) a mixer with a pMOS switch circuit tuned by an inductor. For comparison under the same conditions, cell sizes of the transconductance and the LO switch stages are equal for the mixers. The same tail current source, load resistance, and bias, such as gate-source voltage (V_{gs}) of the transconductance stage and the LO switch stage, are also applied. Both the transconductance and LO switch stage cells width/length are 129.6 μ m/0.13 μ m, resistance of the load is 200 Ω , and the degeneration inductor is 4.2 nH. Size of the pMOS switch cell width/length is 18 μ m/0.13 μ m without the inductor and 54 μ m/0.13 μ m with the inductor (11.6 nH), which is the optimum size. These mixers are fabricated and compared for the noise figure and linearity. Fig. 7 shows photographs of the fabricated CMOS mixers using a 0.13- μ m RF CMOS process. Core chip areas without the pads are 0.53 × 0.6 mm² in the conventional Gilbert mixer, 0.53 × 0.6 mm² in the mixer with the pMOS switch circuit, and 0.56 × 0.87 mm² in the mixer with the pMOS switch circuit tuned by the inductor. However, the chip sizes can be reduced further by proper layout. To test the chips, an evaluation chip board is fabricated using an FR-4 printed circuit board (PCB) and the chips are directly mounted on the ground plate of the evaluation boards. To measure RF performances, a two-tone test is performed at 2.4- and 2.401-GHz frequencies. The LO frequency is set to 2.395 GHz in an input power of 5 dBm, while the output signal is measured at an IF of 5 MHz. We apply $V_{gs} = 1.05$ V in the LO switch stage and $V_{gs} = 0.75$ V in the transconductance stage at $V_{dd} = 1.5$ V. Fig. 8 shows the measured fundamental and third harmonic frequency voltages as a function of the differential RF input power swing. The measured IIP3 of the conventional Gilbert mixer is 3.8 dBm. The linearity of the mixer using the pMOS switch circuits is reduced to 2.7 dBm. The mixer using the pMOS switch circuits with the inductor has an IIP3 of 4.4 dBm. Each type of mixer is measured for a single-sideband (SSB) noise figure. Fig. 9 shows the measured and simulated SSB noise figure over the output frequency range from 100 kHz to 100 MHz. The measured SSB noise figure at 1 MHz is 21.7 dB for the conventional Gilbert mixer and is improved to 19.7 dB with the pMOS switch circuits. The proposed circuit has an SSB noise figure of 13.2 dB. These measured data are summarized in Table II.

IV. CONCLUSIONS

A new circuit to improve noise figure and linearity of a Gilbert mixer has been proposed. The pMOS switch circuits sharpen on/off transition of the switching core and flicker noise from the stage is reduced, resulting in an improved noise figure. However, when the circuit is employed in a conventional Gilbert mixer, improvement of the noise figure is limited due to the leakage path through nonlinear capacitances of the pMOS switch circuits. We have employed an inductor to tune out the path and can efficiently insert the current for further improvement of the noise performance. The linearity degradation due to the nonlinear capacitances of the pMOS switch cell is also reduced by using the resonant circuit. Consequently, the proposed Gilbert mixer improves the noise figure and linearity. We have demonstrated the improved performance of the proposed mixer using a 0.13- μ m CMOS process.

ACKNOWLEDGMENT

Fabrication of the chip was supported by the Samsung Electronics Company Ltd., Yongin, Gyunggi, Korea.

REFERENCES

- [1] M. D. Jamal and A. F. Tor, *CMOS RF Modeling, Characterization and Applications*. Singapore: World Sci., 2002.
- [2] B. Gilbert, "A precise four quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. SC-3, no. 12, pp. 365–373, Dec. 1968.
- [3] P. J. Sullivan, B. A. Xavier, and W. H. Ku, "Low voltage performance of a microwave CMOS Gilbert cell mixer," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1151–1155, Jul. 1997.
- [4] T. Melly, A.-S. Porret, C. C. Enz, and E. A. Virroz, "An analysis of flicker noise rejection in low-power and low-voltage CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 102–109, Jan. 2001.
- [5] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, Jan. 2000.
- [6] M. T. Terrovitis and R. G. Meyer, "Noise in current-commutating CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 2917–2924, Jul. 2006.
- [7] H. Kim, S. Ryu, Y. Chung, J. Choi, and B. Kim, "A low phase noise CMOS VCO with harmonic tuned LC tank," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 12, pp. 2628–2632, Dec. 2005.
- [8] H. Darabi and J. Chiu, "A noise cancellation technique in active RF-CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2628–2632, Dec. 2005.
- [9] B. Gilbert, "The micromixer: A highly linear variant of the Gilbert mixer using a bisymmetric class-AB input stage," *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1412–1423, Sep. 1997.
- [10] S. Kang, B. Choi, and B. Kim, "Linearity analysis of CMOS for RF application," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 972–977, Mar. 2003.

- [11] J. Kang, J. Yoon, K. Min, D. Yu, J. Nam, Y. Yang, and B. Kim, "A highly linear and efficient differential CMOS power amplifier with harmonic control," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1314–1322, Jun. 2006.
- [12] J. Vuolevi and T. Rahkonen, *Distortion in RF Power Amplifiers*. Norwood, MA: Artech House, 1999.
- [13] W. Piet and S. Willy, *Distortion Analysis of Analog Integrated Circuits*. Norwell, MA: Kluwer, 2001.
- [14] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998.



Jinho Yang received the B.S. and M.S. degrees in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2005 and 2007, respectively.

In 2007, he joined SK Telecom, Seoul, Korea, where he is currently a Manager of the Access Network Development Team. His research interests include the Universal Mobile Telecommunications System (UMTS) access network, optimization of wireless network, and next-generation communication system (LTE, HSPA+).



Hyejeong Song was born in Daegu, Korea, in 1982. She received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, Korea, in 2006, and she is currently working toward the M.S. degrees in electrical engineering at Pohang University of Science and Technology (POSTECH), Pohang, Korea.

Her interests include CMOS RF circuits for wireless communications, high-frequency analog circuit design, and mixed-mode signal-processing IC design



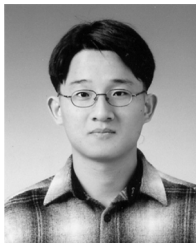
Jehyung Yoon (S'07) was born in Seoul, Korea, in 1977. He received the B.S. degree in electrical and electronics engineering from Chung Ang University, Seoul, Korea, in 2004, the M.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2006, and is currently working toward the Ph.D. degree in electronic engineering at POSTECH.

His research interests CMOS RF circuits and high-frequency analog circuit design for wireless communications.



Sekyeong Lee was born in Seoul, Korea, in 1977. He received the B.S. degree in electrical engineering from Myeongji University, Kyunggi-Do, Korea, in 2003, the M.S. degree in metallurgical engineering from Yonsei University, Seoul, Korea, in 2005, and is currently working toward the Master degree at the Graduate School for Information Technology, Pohang University of Science and Technology (POSTECH), Pohang, Korea.

His research interests RF broadband low-noise amplifier (LNA) design by using CMOS.



Huijung Kim received the B.S. and Ph.D. degrees in electronic engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2000 and 2007, respectively.

In 2007, he joined the Samsung Electronics Company Ltd., Yongin, Gyunggi, Korea, where he is currently a Senior Engineer involved in the design of RF CMOS receivers for wireless digital video broadcasting system. His interests include CMOS RF circuits for wireless communications, high-frequency analog circuit design, and mixed-mode

signal-processing IC design.



Bumman Kim (M'78–SM'97–F'07) received the Ph.D. degree in electrical engineering from Carnegie-Mellon University, Pittsburgh, PA, in 1979.

From 1978 to 1981, he was engaged in fiber-optic network component research with GTE Laboratories Inc. In 1981, he joined the Central Research Laboratories, Texas Instruments Incorporated, where he was involved in development of GaAs power field-effect transistors (FETs) and monolithic microwave integrated circuits (MMICs). He developed a large-signal model of a power FET, dual-gate FETs for gain control, high-power distributed amplifiers, and various millimeter-wave MMICs. In 1989, he joined the Pohang University of Science and Technology (POSTECH), Pohang, Korea, where he is a Namko Professor with the Department of Electrical Engineering, and Director of the Microwave Application Research Center, where he is involved in device and circuit technology for RF integrated circuits (RFICs). He was a Visiting Professor of electrical engineering with the California Institute of Technology, Pasadena, in 2001. He has authored over 200 technical papers.

Dr. Kim is a member of the Korean Academy of Science and Technology and the Academy of Engineering of Korea. He was an associate editor for the *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES* and a Distinguished Lecturer of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S).



Changjoon Park (S'07) received the B.S. degree in materials science and electronic and electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2003, and is currently working toward the Ph.D. degree in electronic engineering with POSTECH.

His interests include digital RF sampling circuit for software defined radio (SDR) systems, RF identification (RFID), CMOS RF circuits for wireless communications, high-frequency analog circuit design, and mixed-mode signal-processing IC design