

A NOISE OPTIMIZED PASSIVE MIXER FOR CHARGE-DOMAIN SAMPLING APPLICATIONS

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Abstract—This paper presents a circuit design technique, based on a CMOS charge-domain passive mixer, for WLAN applications in a 2.4 GHz band. The CMOS passive mixer is designed to mitigate the critical flicker noise problem that is frequently encountered in constitution of direct conversion receivers. The charge-domain method is employed to improve the high frequency performance and noise characteristic. The designed circuit is composed of a trans-conductance amplifier and a passive mixer with a capacitive charge storing load. Fabricated in 0.13 μm CMOS process, this charge-domain mixer achieves a low flicker noise with corner frequency of under 100 kHz, 8.1 dB noise figure, 10.6 dB conversion voltage gain, 2.5 dBm IIP3, and -5.7 dBm P1dB with 2.4 GHz LO driving at 5 dBm. It consumes 4.31 mA from 1.5 V supply.

1. INTRODUCTION

A major challenge in the wireless industry is the high level integration of functional blocks using the low cost CMOS technology. For the single chip radio integration, most of the receiver systems change from heterodyne receiver systems to direct conversion receiver (DCR) systems because of the simple circuit configuration and multi-band integration capability [1–4]. Although the CMOS process has the processing merits of low cost and high integration, it is difficult to design a radio frequency integration circuit using the CMOS process due to its poor noise performance. As CMOS down-scaling progresses, the flicker noise level of the small size transistors tends to increase, and the $1/f$ noise in the DCR systems is a big problem. In order to reduce the flicker noise in the DCR systems, many system designers

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use the passive mixer, which has no DC bias current and has low noise characteristic [5–11]. In a deep sub-micron CMOS process, the time domain resolution of a digital signal edge transition is superior to the voltage resolution of analog signals [12, 13]. Therefore, the discrete-time sampling techniques are a favored solution now for the charge-domain passive mixer based on the digital signal edge transition, and it is an important research topic. As the CMOS process is scaled down for the high integration and high speed operation, the study for the charge-domain sampling technique is progressing rapidly to get the full benefit of the scaling. It is known that the charge-domain sampling technique is better than the voltage-domain sampling technique in high frequency performance, clock feed-through, clock jitter, and noise characteristic [14, 15]. To get the full benefit of the sampling mixer, we have developed the charge-domain mixer with reduced noise.

In this paper analysis of the effects of bias voltage on the thermal noise of the charge-domain passive mixer is presented. The results of the presented analysis are confirmed by Matlab simulation. We also design a passive mixer which is based on a charge-domain. The IEEE 802.11b and 802.11g wireless local area network (WLAN) standards in the 2.4 GHz band are chosen as a target for the implementation. The test chip is designed in a 0.13- μm CMOS technology and includes the trans-conductance amplifier and a bias circuit.

The organization of the paper is as follows; Section 2 presents the noise characteristic of the passive mixer with the bias voltage. In Section 3 the charge-domain passive mixer chip design is described. The simulation and measurement results are also covered in Section 3, and the research efforts of this project are concluded in Section 4.

2. NOISE GENERATION OF THE PASSIVE MIXER

2.1. Thermal Noise

The thermal noise of the passive mixer has been analyzed by M. F. Chang [5] and A. A. Abidi [9]. The voltage-domain and charge-domain passive mixers are similar in thermal noise behavior because the noise sources of the mixers are the same, the drain-source conductance, although the conversion gains of the mixers are not equal. We have analyzed the noise of the charge-domain passive mixer in similar way with the above references.

The conversion gain of the charge-domain passive mixer is given by

$$A_i \approx \frac{\Delta t}{C_L} \text{sinc}(f_{RF}\Delta t), \quad (1)$$

where Δt is the time during the input current charges staying at the load capacitor, C_L and f_{RF} is the input frequency [14]. When the Chang’s method is applied to the noise analysis of the charge-domain mixer, modified conversion gain is

$$A_m \approx \frac{\Delta t}{C_L} \text{sinc}(f_{RF}\Delta t) \frac{T}{\Delta T} \sin\left(\frac{\Delta T}{T}\pi\right), \tag{2}$$

where

$$\Delta T = \frac{\int_0^T g(t)dt}{\mu_n C'_{OX} \frac{W}{L} V_c},$$

g is the drain-source conductance of the transistor, μ_n is the mobility of the electron, W and L is the width and length of the transistor, $V_c = V_{LO} - V_b - V_{th}$, V_b is the bias voltage and T is the period of V_{LO} . The noise figure (NF) of the charge-domain passive mixer is given by

$$NF = 1 + \frac{4kT/g}{4kTR_S} \frac{1}{A_m^2} = 1 + \frac{\pi^2 \Delta T}{4T g_{max} R_S} \frac{1}{A_i^2 \sin^2\left(\frac{\Delta T}{T}\pi\right)}. \tag{3}$$

The noise behavior of the passive mixer using the Eq. (3) is shown in Fig. 1. We know that the noise of the charge-domain passive mixer is related to the bias voltage through V_c . The larger the amplitude of LO signal, A_{LO} , is and the lower the bias voltage is, the better the noise performance is. But the bias voltage has the minimum limit because the output stage of the passive mixer is connected to an opamp for impedance conversion. The minimum value of the bias voltage is about 0.3 V, which is the minimum operating voltage of the output stage opamp. As the result of these conditions, we choose the bias voltage of 0.35 V to improve the noise performance, and then V_c is 0.25 V.

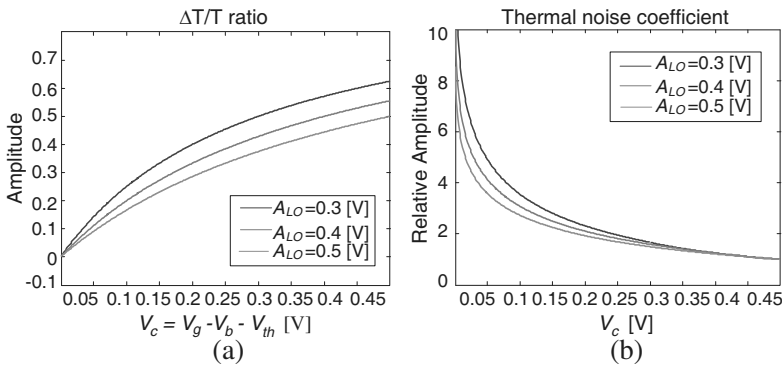


Figure 1. MATLAB simulation results with the bias voltage, (a) $\Delta T = T$ ratio, (b) noise figure.

2.2. Flicker Noise

A low flicker noise is one of the merits of the passive mixer. The flicker noise is given by

$$V_n^2 = \frac{k}{C_{OX}WL} \cdot \frac{1}{f},$$

where k is a fitting factor. Theoretically, there is no flicker noise in passive mixer because there is no DC current source. But it is found that the flicker noise exists in the circuit. According to Abidi [9], the flicker noise on the passive mixer is given by

$$V_{no} = \frac{A}{(S \cdot T)_{LO}} \left(\sum \mp v_n(f \pm f_{in} - 2nf_{LO}) \right) \quad (4)$$

where A is the amplitude of the input signal, S is the slope at commutation and $v_n^2(f)$ is the spectral density of the gate-referred noise of MOSFET.

If there is an interferer at $f_{in} + f_{LO}$ or $3f_{LO} - f_{in}$, we can find a flicker noise at the signal baseband. Therefore, it is possible to suppress the flicker noise of the passive mixer by applying a large blocking at $2f_{LO}$. One of the methods that can be applied for a large blocking at $2f_{LO}$ is the quadrature charge-domain sampling technique [16]. It also helps to reduce the thermal noise of the passive mixer [14]. We have applied this technique to the designed mixer.

3. IMPLEMENTATION AND MEASUREMENT RESULTS

The circuit topology of the charge-domain passive mixer is consisted of a trans-conductance amplifier (TA), a passive mixer with charging storage capacitance, and a bias circuit. For the charge-domain operation, the TA block creates the current. We have designed a passive mixer with good noise performance using the bias voltage control method mentioned in Section 2.

The TA, which operates at 2.4 GHz, is composed of the push-pull type inverter circuits shown Fig. 2(a). The linearity of the TA is enhanced by increasing the g_m and reducing the IM_3 component using a multi-gate bias method. The main block of this circuit consumes only 3.87 mA with 1.5 V supply. An additional current of 0.4 mA is used for the multi-gate bias operation. The designed passive mixer is shown in Fig. 2(b). It has an ac coupling capacitor to overcome the DC offset problem in RF input part, and it does not use any dc bias current to decrease the flicker noise. It is designed for a quadrature sampling structure to obtain additional filtering effect at $2f_{LO}$. The

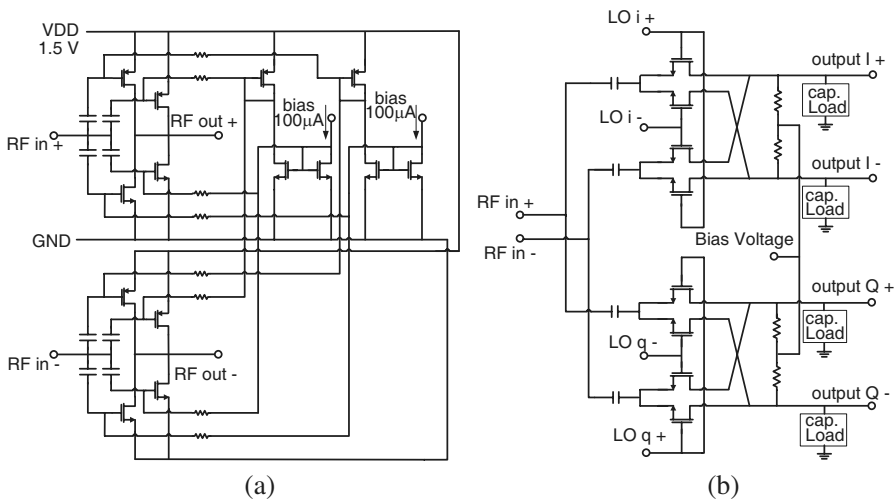


Figure 2. Schematic of the proposed circuit, (a) trans-conductance amplifier, (b) passive mixer.

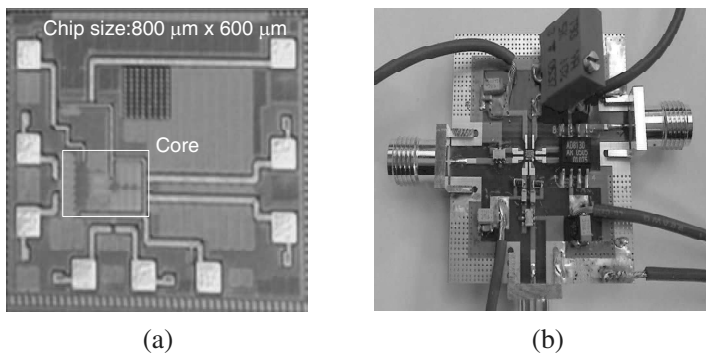


Figure 3. Designed circuit in 0.13 μm CMOS process, (a) micrograph, (b) PCB for the chip test.

bias voltage are selected as 0.35 V, not a half of the supply voltage, for improvement of the thermal noise performance.

The proposed circuit is fabricated using 0.13 μm CMOS process. A die photograph of the designed circuit is shown in Fig. 3 with size of $800 \times 600 \mu\text{m}^2$. The core size, except the PAD, is $300 \times 350 \mu\text{m}^2$. The performance of the proposed circuit is verified by testing the differential system. We use 1:1 impedance matching balun which operates at 2.4 GHz to measure the differential input system, and use the AD8130

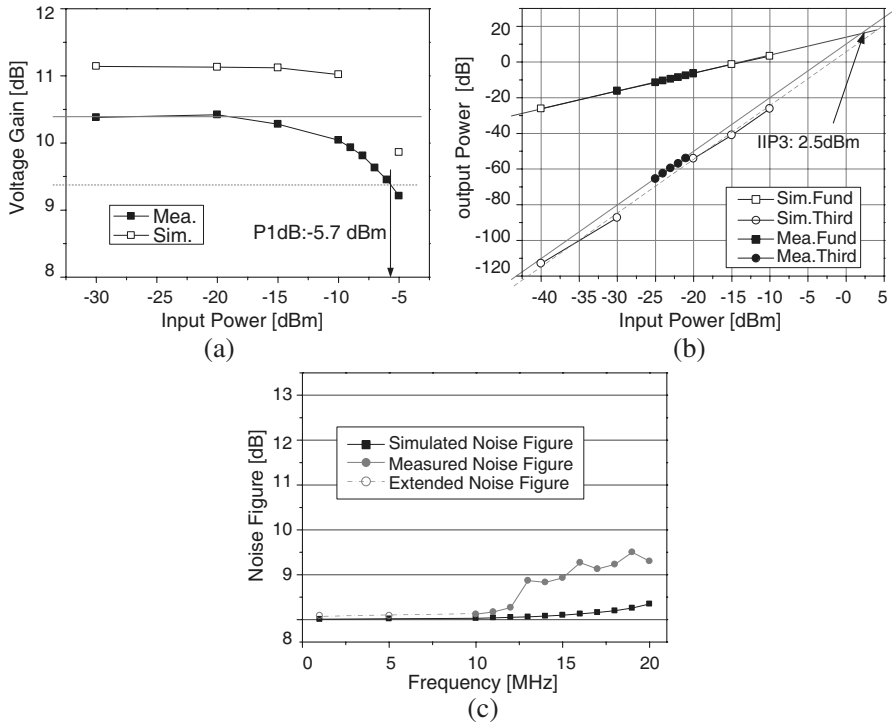


Figure 4. Simulation and measurement results of the designed circuit, (a) P1dB, (b) IIP3, (c) noise figure.

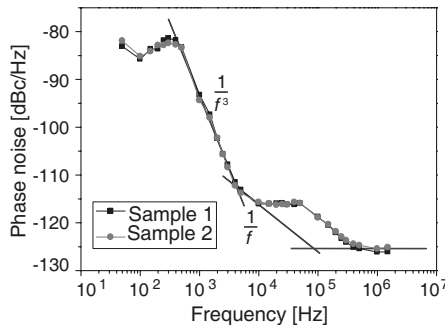


Figure 5. Measured flicker noise results of the designed circuit.

Opamp to measure the differential output system. The circuit is biased at 4.31 mA with 1.5 V supply. The simulation and measurement results of the circuit are plotted in Figs. 4 and 5. To measure the IIP3, two-

Table 1. Summary of the measured performance of this work and comparison to others published data.

	This work	[17]	[18]
Supply Voltage [V]	1.5	1.8	1.2
DC Current [mA]	4.31	4.5	4.8
Conversion Gain [dB]	10.6	15.7	8.2
P1dB [dBm]	-5.7	-	-
IIP3 [dBm]	2.5	1	-0.3
Noise Figure @ 1MHz [dB]	8.1	12.9	9.6
1/f noise corner frequency [kHz]	100	-	-

tones with frequencies $f_{in_1} = 2.401$ GHz and $f_{in_2} = 2.4014$ GHz were applied at the input. Then, the measured P1dB and IIP3 are -5.7 dBm and 2.5 dBm, respectively. In case of noise power measurement, we test the fabricated circuit from 10 MHz and up because the equipment does not measure noise power under the 10 MHz and the result is shown in Fig. 4(c). The measurement result of the flicker noise is shown in Fig. 5. It exhibits 8.1 dB NF and 1/f noise corner frequency under about 100 kHz. The experimental results show that there are no significant performance degradations from the simulation data. The performance of the designed circuit is compared to the other published circuits, and summarized in Table 1 [17, 18]. The designed circuit has the lowest noise figure and the best IIP3 as shown in Table 1.

4. CONCLUSIONS

We have optimized the RF noise performance of a passive mixer, which is normally used to improve the flicker noise performance in DCR structure, by adjusting the bias voltage and adding the charge-domain sampling method. We design the TA for charge-domain operation whose linearity performance is enhanced by IM3 cancelation using multi-gate bias method. The designed TA and mixer exhibits 10.6 dB gain, 2.5 dBm IIP3, -5.7 dBm P1dB, 8.1 dB NF, and low flicker noise of under 100 kHz. One of the key building blocks for SDR receiver system is charge-domain passive mixer explained in this work, and this design method should be helpful to study about the digital RF receiver system.

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