



# Technical Committee News

## TC-Sponsored Contests

### Message from the MTT-S Technical Coordinating Committee Chair

■ Richard V. Snyder

The High-Power Microwave Components Committee (MTT-5) has held a student-based high-efficiency power amplifier (PA) design contest since 2005. This allows students to focus not only on the theory of the amplifier but also provides hands-on involvement in the practical implemen-

tation. The contest has been well received by many engineering students and Microwave Theory and Techniques Society (MTT-S) members. Last year, the IEEE MTT-S Technical Coordinating Committee (TCC) decided to extend the contest to all MTT-S technical committees (TCs)



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on a regular basis to provide a forum for two-way information flow between the expert members of the TC and the general MTT-S membership.

## MTT-5 Student High-Efficiency PA Design Competition

■ Jim Komiak, Past Chair MTT-5 High-Power Amplifiers

Despite the growing importance of radio frequency (RF) and microwave technology in our lives, its study has not attracted the attention it should. Engineering students have favored computer and digital electronics, and the number of university students interested in RF and microwave technology has declined despite high demands in the job market. The lack of new graduates with appropriate skills has been recognized

by government, industry, and academia. After much discussion, TCC MTT-5 High-Power Amplifiers decided to initiate a Student High-Efficiency PA Design Competition at IMS2005 Long Beach, CA in the hope that this exciting challenge would produce additional educational interest and the rewards of building experimental prototypes. The student response has exceeded our expectations with the number of entries increasing every

year. The contest will again be held for the fifth year at IMS2009 Boston, MA.

A paper authored by the winner of the IMS2008 Atlanta, GA competition describing the theory behind and the experimental results of their entry is presented in this issue. The concept of student design completions has been expanded to an initiative to bring something similar to all the TCs of the MTT-S.

# A Saturated PA with High Efficiency

■ Jangheon Kim, Junghwan Moon, Bumman Kim, and Raymond S. Pengelly

The IEEE MTT-5 student design competition for high-efficiency PAs provides the opportunity for the student to do an in-depth study of a PA from theoretical concept and analysis to fabrication and testing. This competition motivates many students to have a strong interest in a highly efficient PA design and development. The contest rules require the PA to operate at a frequency greater than 1 GHz but less than 20 GHz and produce an output power of greater than 5 W but less than 100 W into a 50  $\Omega$  load with a power input of less than 25 dBm. A participant demonstrates the PA at the International Microwave Symposium (IMS), and the designer of the PA with the highest power-added efficiency (PAE) becomes the winning entry of the contest. The PAs designed by previous winners showed PAE with >75% at about 1 GHz frequency range [1]–[3]. In the 2008 contest, a new rule, which has a frequency weighting factor of the PAE multiplied by (GHz)<sup>0.25</sup>, was introduced to encourage PA design at higher frequencies.

This article presents the design of the winning PA with PAE of 73.2% at 3.2 GHz operating frequency, which is equivalent to the weighted PAE performance of 97.9%. It will be shown that the saturated PA, which has a high fundamental load impedance considering the knee region of the transistor, can generate high efficiency even in the high-frequency region. An overview of the saturated operation behavior, design, and implementation is presented here along with the experimental results.

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## Planning for the Competition

The performance of last year's winning PA was excellent, about 83% PAE at 1.2 GHz frequency. To differentiate our PA from the other PA designs, our main strategy was to maximize PAE at a higher frequency. Thus, we have explored a high-frequency device and have chosen a gallium nitride (GaN) high-electron-mobility transistor (HEMT) from Cree because the device provides a high gain characteristic up to 4 GHz operation. In addition, a medium-power device (CGH40010) with a 10 W output was used because the input level rule limits the input drive to less than 25 dBm, and we wanted to drive the device into saturation for high efficiency.

Last year's winning PA was focused on optimizing the PA using electromagnetic (EM) simulation [3]. That is not enough for us because we want to design a high-efficiency PA at a high frequency. We focused on the study of the basic PA theory and development of the PA design scheme based on the reported papers. We tried to design a standard PA such as class-E and class-F to achieve high efficiency, but it is difficult to control harmonic content in the higher-frequency regime. For example, a 3 GHz class-F amplifier requires zero impedance at the second harmonic of 6 GHz and high impedance at the third harmonic of 9 GHz. The harmonic tuning

impedance should be provided at the current source of the device together with the power matching at the fundamental frequency. It is hard to deal with the high harmonic impedance termination because of the large output capacitance of high-power devices. As a result, a design strategy that is different from the general high-efficiency PA design scheme should be considered.

## Saturated Operation with Large Fundamental Load Impedance

The basic concept of the high-efficiency PA design in the high-frequency region is to control the first few harmonics to minimize internal power consumption of the transistor, but the matching topology of the PA should be easily realizable [4]–[6]. The potential of second harmonic termination was investigated by Paolo Colantonio [7], [8] to achieve high efficiency. The idea of the investigation is that the second harmonic termination induces a voltage reduction in the lower half of the quasi-half-sinusoidal shape, while the voltage is enhanced in the upper half. From the voltage reduction, the overlap between the current and voltage waveforms is minimized. As a result, the internal power consumption is reduced and the efficiency is improved. We have extended this idea to the saturated PA operation for

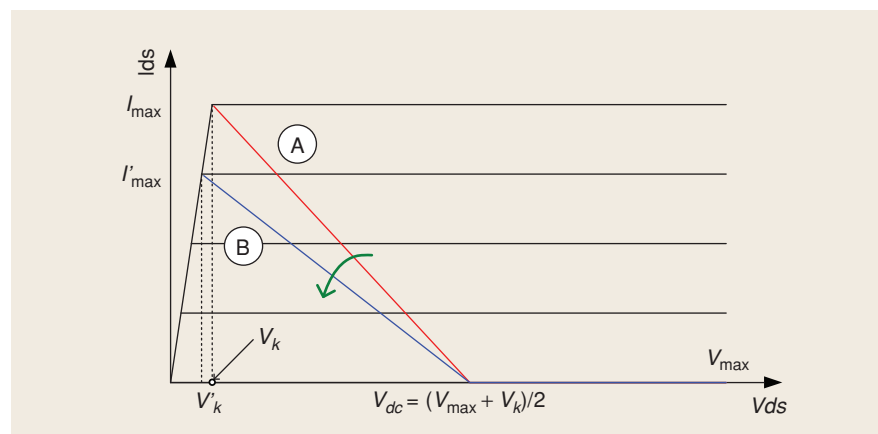


Figure 1. Load-line trajectories according to the fundamental load impedance for class-B PA.

enhanced efficiency. While saturated operation in the knee region generates the second harmonic current, the voltage waveform is properly shaped by the appropriate second harmonic termination. The large fundamental load impedance, higher than that of a general PA, is employed to increase the power gain at high frequencies.

The load lines of a class-B PA, for various magnitudes of the fundamental load impedances, are shown in Figure 1. The efficiency  $\eta$  and PAE  $\eta_{\text{add}}$  of the PA with the proper fundamental load impedance are defined as

$$\begin{aligned}\eta &= \frac{P_{\text{RF}}}{P_{\text{dc}}} = \frac{1}{2} \frac{I_{\text{fund}} V_{\text{fund}}}{I_{\text{dc}} V_{\text{dc}}} \\ &= \frac{\pi}{4} \frac{V_{\text{max}} - V_k}{V_{\text{max}} + V_k} \\ \eta_{\text{add}} &= \eta \times \left(1 - \frac{1}{G}\right) \\ &= \eta \times \left(1 - \frac{w^2 C_{gs}^2 R_{in}}{g_m^2 R_L}\right)\end{aligned}\quad (1)$$

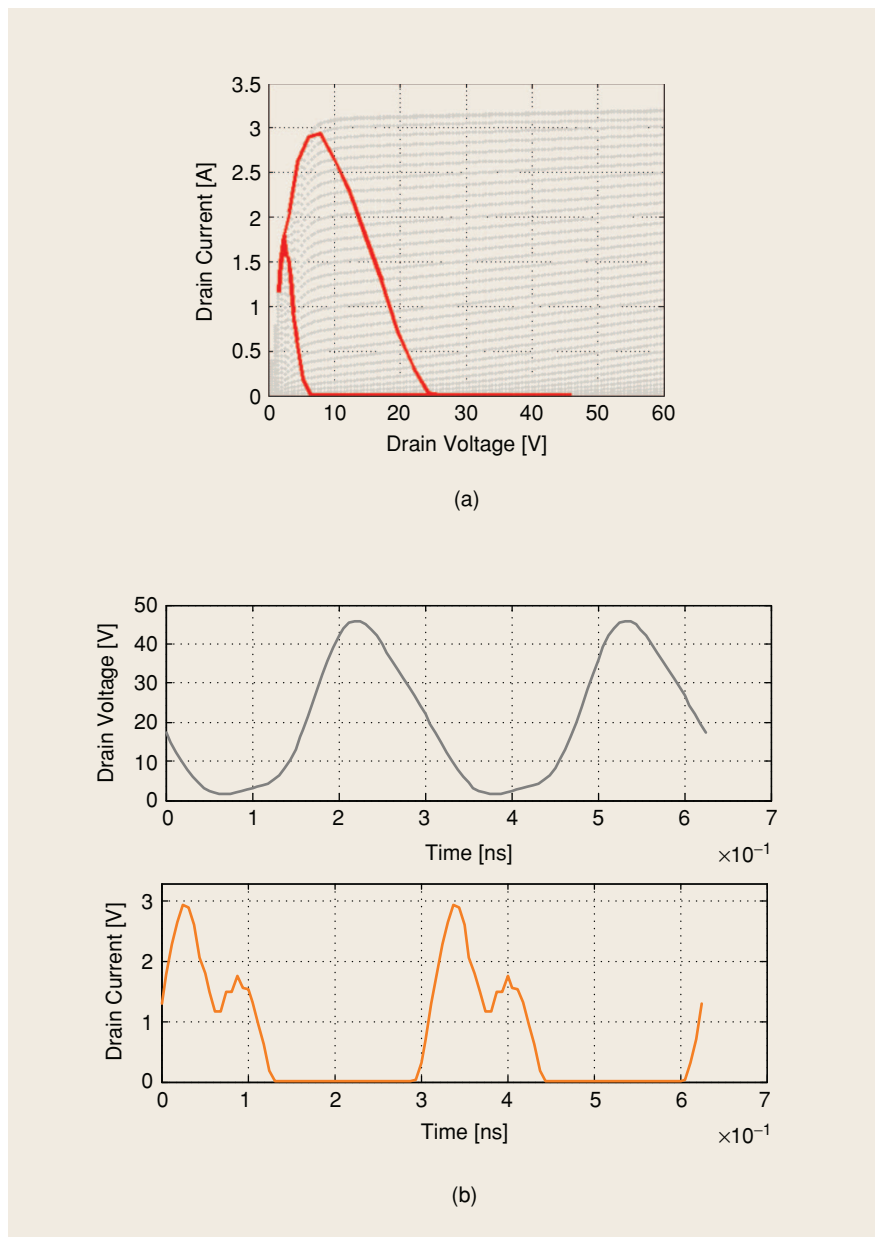
where  $P_{\text{RF}}$  and  $P_{\text{dc}}$  are RF and dc powers, respectively.  $I_{\text{fund}}$  and  $V_{\text{fund}}$  are fundamental current and voltage components, respectively.  $I_{\text{dc}}$  and  $V_{\text{dc}}$  are dc

current and voltage components, respectively.  $I_{\text{max}}$  is the maximum current,  $V_{\text{max}}$  is the maximum voltage, and  $V_k$  is the knee voltage [9]. As the load impedance is increased, the load line moves down (from A to B in Figure 1) so that the knee voltage is reduced. Although the output power is reduced for the large fundamental load impedance, the efficiency is increased due to the reduced knee voltage. In addition, the power gain of the PA is increased, enhancing the PAE, so this design approach is appropriate for high-frequency operation. In saturated operation with the large fundamental load impedance, second and third harmonic current components are generated at the device. The current components shape the voltage waveform at the output load with harmonic control.

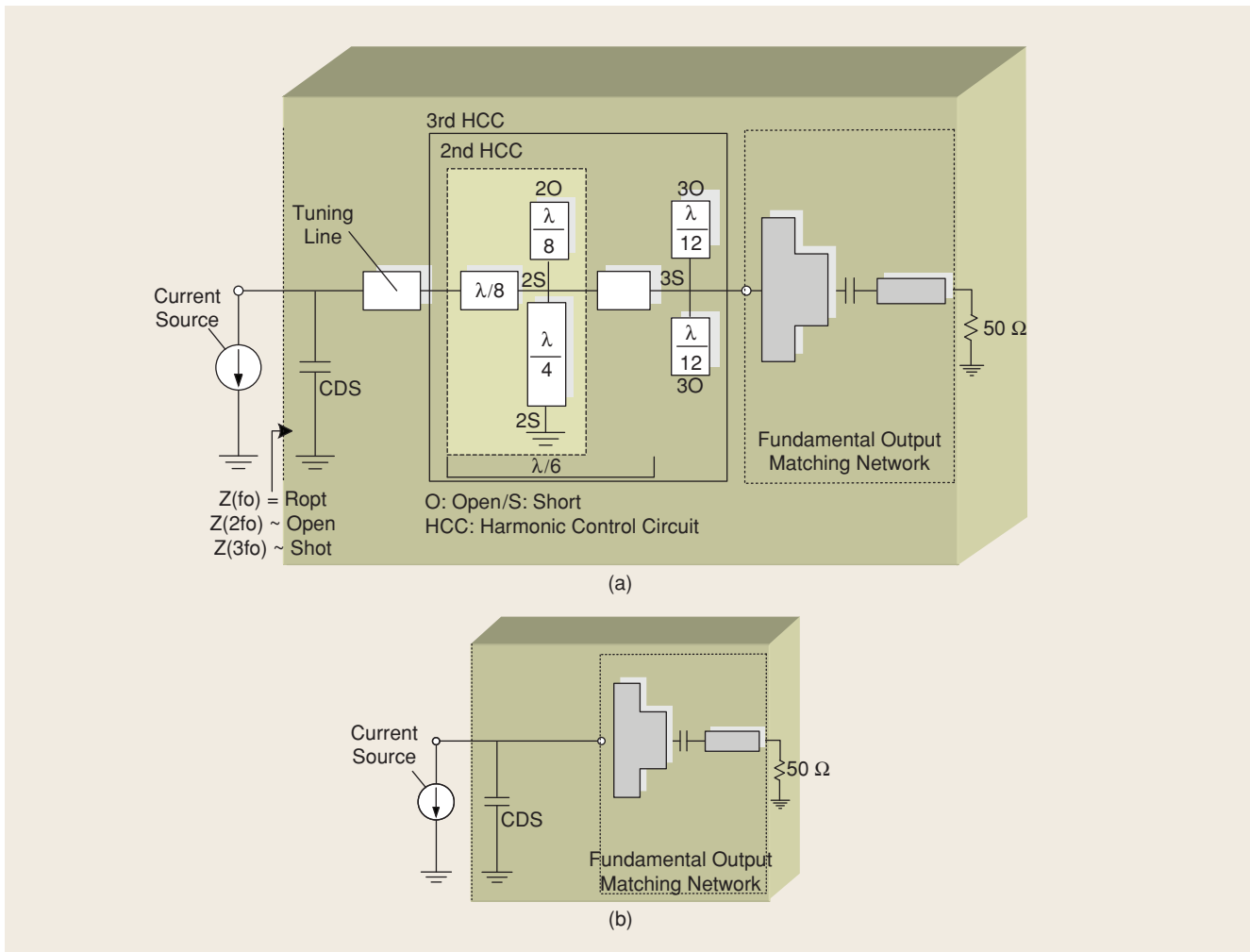
The load-line trajectory and the saturated current and voltage waveforms for the best efficiency are simulated using the Cree model of the CGH40010 device, as shown in Figure 2(a) and (b). The load line trajectory depicts the triangular looping curve with saturated operation in the knee region, indicating that there is an imaginary part in the load. The generated third harmonic current component changes the half-sinusoidal current waveform into a quasi-square waveform. Also, the quasi-half-sinusoidal voltage waveform with voltage peaking is produced by the second harmonic current with the appropriate second harmonic termination. Building complex or imaginary second harmonic terminations is required, as indicated in [4]–[8]. These waveforms produce the minimized overlap between the current and voltage waveforms and are similar to the waveforms of an inverse class-F PA.

Figure 3(a) shows the simplified schematic diagram of a conventional inverse class-F PA output matching network that includes the harmonic loading circuit for the second and third harmonic terminations presented in [2]. There is a tuning line to compensate the  $C_{\text{DS}}$  output capacitor.

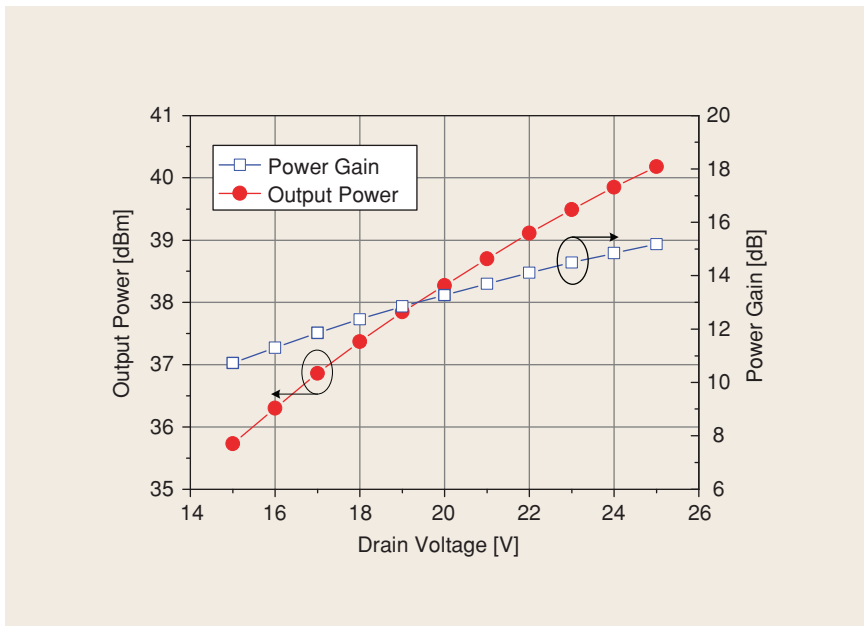
Figure 3(b) shows the simplified schematic diagram of the proposed output matching network. This circuit topology, employed by the  $C_{\text{DS}}$  output



**Figure 2.** Simulated (a) load line and (b) current and voltage waveforms. In the simulation environment, the PAE is 72.3% at an output power of 38.3 dBm.



**Figure 3.** Simplified schematic diagram of (a) conventional inverse class-F output matching network and (b) proposed output matching network.



**Figure 4.** Measured output power and power gain according to the drain voltage for an input power of 25 dBm.

capacitor of the device along with the fundamental matching circuit, provides not only the proper load impedance for the second harmonic frequency but also the proper low impedance for the third harmonic frequency. In this matching circuit, the second harmonic impedance is not high in comparison with the open impedance of the conventional design because of the high second harmonic current generation from saturated operation. This design approach shows the potential of realizing a highly efficient PA using a simple matching topology with a low loss compared to the previously reported results [2], [10]–[12].

### Implementation and Experimental Results

In order to maximize the weighted frequency PAE of the competition rules,

the PA should be operated at a high frequency, and the high-power gain should be obtained at this frequency. In particular, it is important to design for high power gain because the input power level is limited to 25 dBm, while the smallest GaN device we can get has 40 dBm output power. Thus, the PA is designed for an output power of >38 dBm (the minimum power gain is 13 dB) and a drain efficiency of >75% (the target PAE is approximately 72%) at an operating frequency of 3.2 GHz (weighted frequency factor is about 1.3). The goal for the competition was to achieve a weighted efficiency of >90% because we thought that the majority of participants operate at 2 GHz frequency (weighted frequency factor is of 1.2) and it is difficult to achieve PAE of >75% at 2 GHz.

The PA is designed using the Cree CGH40010 with 10 W saturated output power. The transistor used is available in a screw-down package and does not include any internal matching circuit. The simulation and layout of the amplifier are performed using Agilent Advanced Design System (ADS) and MATLAB software. The amplifier is implemented with a TACONIC TLY board to minimize the input and output matching losses, which have a low-loss characteristic of 0.005 loss tangent at 3.2 GHz ( $\epsilon_r$  is 2.2 and height is 31 mil). The PCB board is fabricated in the etching facility at Pohang University of Science and Technology (POSTECH). The small aluminum jig was fabricated in the machine shop. The testing and performance analysis of the amplifier were performed with the power measurement setup in our laboratory, which consists of a signal generator, power meter, spectrum analyzer, and network analyzer.

Figure 4 shows the output power and power gain versus drain voltage at an input power level of 25 dBm, the maximum level for the test in the competition. The measured output power and power gain are about 40 dBm and 15 dB, respectively, at an input power of 25 dBm and drain voltage condition of 25 V. The high gain characteristic of the amplifier is achieved through the

large fundamental load impedance. The efficiency versus the drain voltage, for the testing condition of Figure 4, is illustrated in Figure 5. As shown in this figure, the maximum PAE is achieved around  $V_{ds} = 20$  V, although the output power is reduced. The maximum drain efficiency is obtained at the drain voltage of 17 V. The difference in the optimum drain voltage is related to the low power gain at the low drain voltage (see Figure 4). From this experiment, a drain voltage condition of 20 V is adopted to maximize the PAE. The implemented amplifier is operated at a

quiescent deep class-AB bias with  $V_{GS} = -2.52$  V.

Figure 6 shows the output power and power gain versus input power level for a drain voltage of 20 V. The measured drain efficiency and PAE of the amplifier are also shown in Figure 7. The measured output power and PAE are approximately 38.3 dBm and 73.2%, respectively, at an input power of 25 dBm with a drain voltage of 20 V. The weighted PAE is 97.9% from the measured PAE and operating frequency. A photograph of the implemented PA is shown in Figure 8.

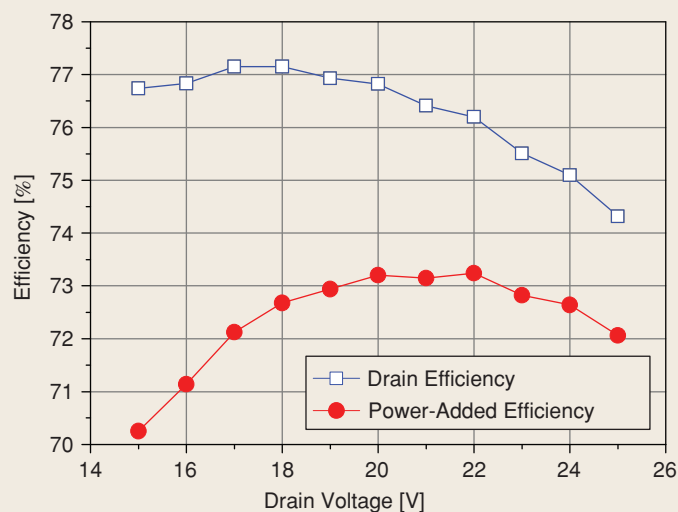


Figure 5. Measured drain efficiency and PAE according to the drain voltage for the input of 25 dBm.

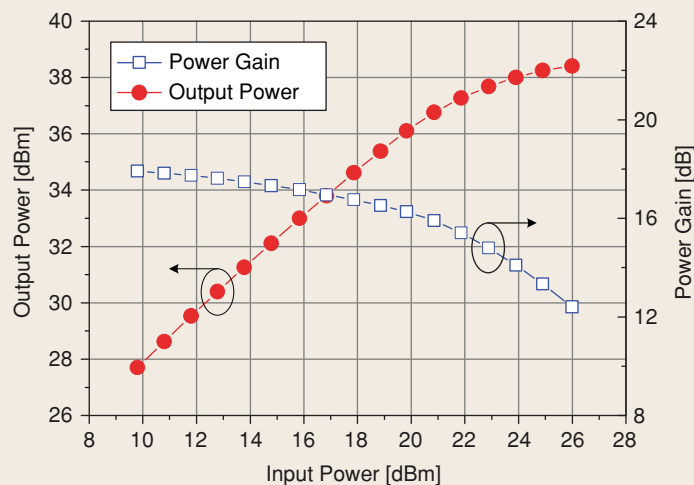


Figure 6. Measured output power and power gain at the drain voltage of 20 V.

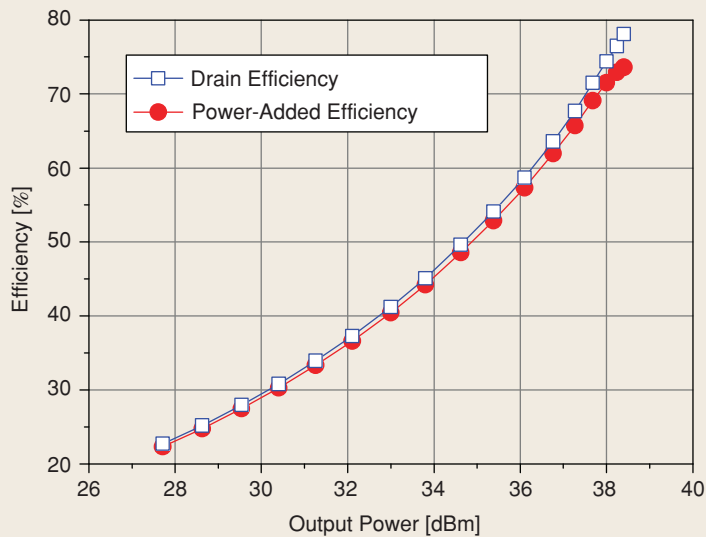


Figure 7. Measured drain efficiency and PAE at the drain voltage of 20 V.

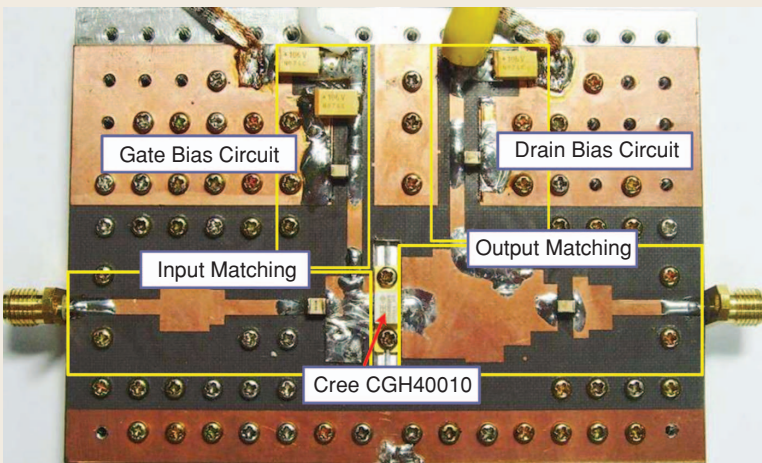


Figure 8. A photograph of the implemented PA.

## Conclusion

A brief design strategy for the competition is presented in this article. The amplifier is designed for saturated operation with high gain at a high frequency to maximize the weighted-frequency PAE. Our work has demonstrated an advanced design method for a PA with high efficiency at high frequency, which is synthesized using appropriate harmonic control without any special harmonic loading circuit for reduced loss. Future studies will

include further examination for saturated operation behavior containing the knee region and investigation of the correlation between the fundamental load impedance and harmonic terminations to achieve high-efficiency performance.

Attending the high-efficiency PA design competition was a great compliment for me, and provided me a good opportunity to communicate with other PA researchers. Through design, fabrication, test, and analysis

of the PA, I really experienced the challenge of high-efficiency PA development, which requires innovative or evolutionary ideas. Also, it provided me an opportunity to learn the new trends in high-efficiency PAs and to collect information about state-of-the-art devices.

I would like to encourage other students to attend this competition because it gives them an opportunity to investigate or demonstrate their innovative ideas for realization of a PA with high efficiency.

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## MTT-6, MTT-16, and MTT-20 Low-Power FM Receiver Contest

■ Roger Kaul, Past Chair of MTT-16 and Chair of UWB Systems Subcommittee

The 2008 IMS featured a student contest designed to emphasize the importance of meeting the design objectives while using the minimum amount of prime (battery) power. The design objective was to receive a commercial stereo FM signal and drive a stereo headphone to a 4 mW peak audio level per channel.

Two students from the University of Cologne won the contest. By using very low-power semiconductor devices, unusual circuitry, and making some of their own components they met the goal while consuming less than 16 mW of power.

2008 was the first year for this contest. The contest was sponsored

by the Microwave and Millimeter-Wave Integrated Circuits (MTT-6), Microwave Systems (MTT-16), and Wireless Communications (MTT-20) TCs. For IMS 2009 we plan to have another student contest involving a 2.45-GHz low-noise amplifier.

## Student Competition for Low-Power Consumption FM Receiver Design

■ Christian Musolff, Andreas Neuberger, and Rainer Kronberger

The objective of the Low-Power FM Radio Receiver contest, held during the IMS 2008 in Atlanta, was to "design, construct, measure, and demonstrate an FM radio receiver with low dc (battery) power consumption driving simple earphones/ear buds." It was further specified that "the LPFMR's performance shall be measured while receiving an FM stereo signal from a local FM station with a peak audio output power of 4 mW per chan-

nel. The performance is based solely on the input power, which shall be computed as the dc supply voltage times the dc supply current."

From the beginning, it was clear for us that a modern implementation of classic circuitry would be unbeatable with respect to power consumption, although that might seem strange. In the 1960s, when transistors were quite expensive, circuitry was well thought out to save on active parts [1]–[4]. A low active part count however results in low power consumption. That seemed to be a firm footing to put the project on. Another point was that we did not want to use fully integrated receiver circuits (e.g., TEA5768HL, TDA7000....), because those parts do not leave much freedom for any engineering challenge,

which, in our opinion, should be the actual sense of such a competition. Commercially available receiver subsystem ICs [e.g., integrated intermediate frequency (IF) amplifiers, stereo decoders] also did not match the demands of very low power consumption. The only integrated circuits used in the design were modern micropower rail-to-rail OpAmps, whose performance is compelling. National's LMV552 (37  $\mu$ A quiescent current per amplifier) was chosen wherever the signal frequency allowed it—thus in all audio stages and in the stereo decoder.

### Circuitry

Figure 1 shows the overall block diagram of the FM receiver, which is based on a standard FM superheterodyne receiver concept, containing a selective

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