

Highly efficient 3-stage Doherty power amplifier using gate bias adaption

ILDU KIM, JUNGHWAN MOON, JUNGJOON KIM, SEUNGHOO JEE, JUNGHWAN SON AND BUMMAN KIM

This paper demonstrates a highly efficient 3-stage Doherty power amplifier (PA) employing an envelope tracking (ET) technique. The '3-stage' Doherty PA is the most efficient architecture for a high peak-to-average power ratio (PAPR) signal among the various Doherty PAs. However, because of the lower peaking biases than those of the 'N-way' Doherty PA, the proper load modulation is hard to be achieved. To get proper modulation, the peaking PAs' gate biases have been adaptively controlled using the ET technique, and the peak power and maximum efficiency characteristic along the backed-off output power region is successfully achieved. By ADS and Matlab simulations, the overall behavior of the 3-stage Doherty PA employing the ET technique has been fully analyzed. To maximize the overall efficiency of the proposed 3-stage Doherty PA, the unit PA has been designed using class F^{-1} PA. For verification, the amplifier is implemented using 5 W and 10 W PEP LDMOSFETs for the 802.16e mobile world interoperability for microwave access (WiMAX) at 1 GHz with a 8.5 dB PAPR. The measured drain efficiency of the proposed 3-stage Doherty PA is 55.5% at an average output power of 37 dBm, which is a 7.54 dB backed-off output power. The digital feedback predistortion (DFBPD) algorithm has been used to linearize the proposed PA considering the ET technique. After linearization, the -33.15 dB of relative constellation error (RCE) performance is achieved, satisfying the system specification. These results show that the 3-stage Doherty employing the ET technique and saturated PA is the most suitable PA for the highly efficient and linear transmitter.

Keywords: RF transmitter, Power amplifier (PA), N-way Doherty PA, 3-stage Doherty PA, Envelope tracking (ET), Power-added efficiency (PAE), Relative constellation error (RCE), Peak-to-average power ratio (PAPR), Efficiency, Linearity, World interoperability for microwave access (WiMAX), Digital feedback predistortion (DFBPD)

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I. INTRODUCTION

For the modulation signal with a high peak-to-average power ratio (PAPR), the transmitter should be operated at a backed-off average output power region for an acceptable linearity, resulting in a low-efficiency characteristic. However, a high efficiency with high linearity is essential for a low-cost wide-band transmitter. To achieve both the requirements at the same time, a combined architecture of an efficiency enhancement technique and a linearization technique should be developed. As a linearization technique, the digital predistortion (DPD) shows a very powerful and reliable linearization capability and is the favored method for the linearization of the base-station amplifier [1]. As an efficiency enhancement technique, the hybrid envelope elimination and restoration/envelope tracking technique (H-EER/ET) and the Doherty technique can be considered [2–9]. Recently, these two techniques delivered an excellent efficiency performance. In the H-EER/ET transmitter, the power amplifier (PA) is driven to the saturated state by the modulated input signal, and the drain bias of the PA is modulated by the optimum envelope signal through the efficient bias modulator. Owing to the

saturated operation along the whole output power level, highly efficient operation can be expected, and high linearity can be achieved theoretically by the separated restoration mechanism of the amplitude and phase information [7, 8]. But the H-EER/ET transmitter is not implemented for the mass production at the industry yet owing to difficulties such as efficiency and bandwidth enhancement of the bias modulator and complexity of the circuit compared to the other PAs. On the other hand, the Doherty technique is not an optimum architecture in terms of efficiency for amplification of a high-PAPR signal, because the efficiency degradation region exists at the low-power region and the unsaturated peaking PA's operation region [3, 10]. In spite of this imperfection, the Doherty PA has been delivering the highest efficiency among various PAs because of the well-developed simple circuit. Accordingly, the Doherty PA market has experienced rapid growth in recent years [11].

In this paper, by considering the distribution of a PA's power generation probability for the modulation signal [12], we have verified that the most efficient Doherty architecture for a high-PAPR signal is the 3-stage Doherty PA. For a highly efficient operation at the backed-off output power region, while maintaining the peak power, we optimized the "ET" 3-stage Doherty PA by using Matlab simulation. The unit PA has been designed using a saturated mode PA to maximize the Doherty PA's efficiency. The 5 W and two 10 W PEP LDMOSFETs are employed for the 802.16e mobile world interoperability for microwave access (WiMAX) signal with 8.5 dB PAPR at 1 GHz.

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II. COMPARISON OF N-WAY VERSUS 3-STAGE DOHERTY PA

As reported in many papers [3, 13], the ‘N-way’ Doherty PA has two maximum efficiency points at the backed-off output power and the peak power, respectively. The back-off level for the first maximum efficiency, $20 \log(1/N)$ [dB], is determined by selecting the peaking PA’s size. On the other hand, the ‘3-stage’ Doherty PA has three maximum efficiency points along the output power level [14]. The back-off levels with the two maximum efficiencies are determined by the two peaking PAs’ size ratio compared to the carrier PA, which is derived in [12], $20 \log(k_1)$ [dB] and $20 \log(k_2)$ [dB]. The k_1 and k_2 are the input power back-off points on the normalized input voltage magnitude. In Table 1, the back-off levels of various Doherty PAs are summarized. In Fig. 1, the efficiency characteristics of various Doherty PAs are illustrated when all the PAs are biased at the class B mode in the ideal condition. There are four kinds of 3-stage Doherty PA and two kinds of N-way Doherty PA with different size ratios between the carrier PA and peaking PAs. The 3-stage Doherty PAs maintain relatively flat and high efficiency along the output power level because of the three maximum efficiency characteristics compared to those of the N-way Doherty PA. To evaluate the average efficiency of each Doherty PA for the 802.16e mobile WiMAX signal with 8.5 dB PAPR, the efficiency is calculated using the following equation [15]:

$$\therefore DE = \frac{\int \text{prob.}(V_{in}) \cdot P_{out}(V_{in}) dV_{in}}{\int \text{prob.}(V_{in}) \cdot P_{dc}(V_{in}) dV_{in}}. \quad (1)$$

The $\text{prob.}(V_{in})$ is the probability of occurrences at V_{in} for the modulated input signal. In this equation, the overall DE is determined by the multiplication of the probability distribution and the power generation terms (P_{out}) at the distribution over the DC power (P_{dc}). The numerator of the above function (probability \times power) is named the power generation distribution (PGD) of the Doherty PA [6]. The distribution indicates the important power generation region for the Doherty operation, and the operation at the region determines the average efficiency. In Fig. 1, PGD is also depicted, and the 3-stage Doherty PA maintains the high-efficiency characteristic broadly at the important operation region, while the N-way Doherty PAs do not. In Table 1, the calculated average efficiencies of each Doherty PA for the WiMAX signal are presented, and the 3-stage Doherty PAs have shown about 10% improved efficiency compared to the N-way Doherty PAs. It is clearly shown that the 3-stage Doherty PA is the most efficient architecture for amplification of the WiMAX signal with 8.5 dB PAPR.

The peaking PAs of the N-way Doherty PA are biased at a class C mode for the proper turn-on operation at the required output power level, and the carrier PA should be driven into hard saturation to achieve its peak power. The peaking PAs of the 3-stage Doherty architecture are turned on one after the other and it is in the worse situation because the PA’s gate bias is lower than that of the N-way Doherty case. Thus, the load cannot be modulated completely at the peak power region, even worse than the N-way Doherty. Because of the incomplete load modulation, we cannot achieve high efficiency and high peak power simultaneously. Therefore, we have to select one of the two design cases. One is the peak power and

Table 1. The back-off level and average efficiency of the ‘N-way’ and ‘3-stage’ Doherty PAs for the 802.16e Mobile WiMAX signal with 8.5 dB PAPR.

		Back-off	DE_{Avg}
■ N-way	Two-way	−6 dB	59%
	Three-way	−9.5 dB	61.2%
■ Three-stage cell size ratio (Car. : Peak. 1 : Peak. 2)			
	1:2:2	−4.44/−9.5 dB	69.8%
	1:2:3	−6/9.5 dB	69.4%
	1:3:3	−4.87/12 dB	70.5%
	1:3:4	−6/12 dB	71%

flat gain response (linear amplitude modulation-amplitude modulation(AM-AM)) with the poor efficiency at backed-off output power region. The other case is a high efficiency at the backed-off output power level with an insufficient peak power and gain flatness. Both the selections are not the optimum design. To overcome this problem, we may employ the uneven input power drive technique [16], but it reduces the linear gain. Moreover, the load modulation is not enough to achieve high efficiency at the backed-off output power level and the peak power at the same time. The other alternative is the gate bias control of the peaking PAs [17, 18]. Generally, the gate bias control of the Doherty PA has been employed for the IM cancellation. In this paper, we have investigated the peaking PA’s gate bias control of the 3-stage Doherty PA for efficiency improvement at the backed-off output power level and the peak power at the same time besides linearization. The architecture of the proposed 3-stage Doherty PA is shown in Fig. 2.

III. ANALYSIS OF THE PROPOSED 3-STAGE DOHERTY PA

A) Conduction angle of each PA versus input voltage magnitude

We conducted the Matlab simulation to analyze the operation of the 3-stage Doherty PA with and without the gate bias

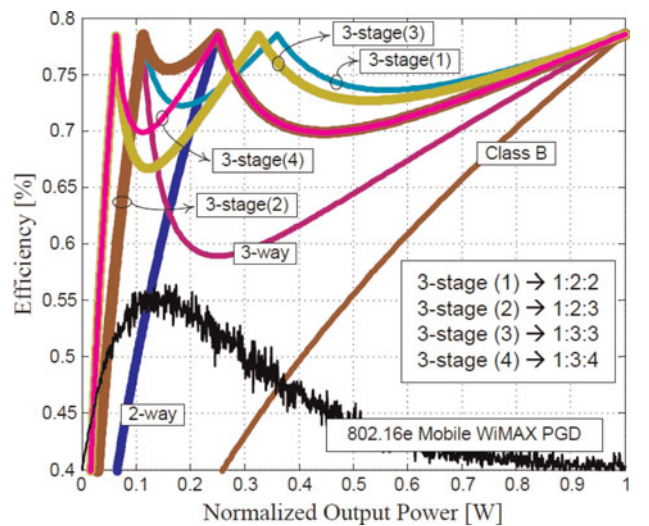


Fig. 1. The efficiency characteristics of various Doherty PA versus the normalized output power.

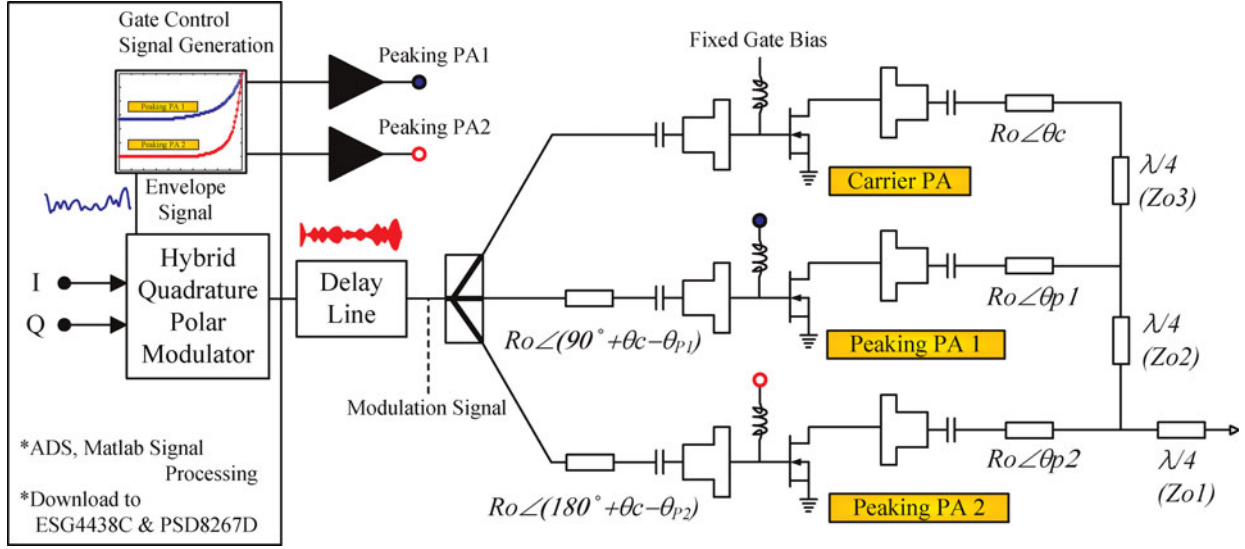


Fig. 2. The architecture of the proposed ET 3-stage Doherty PA.

control. For exact modeling of the peaking PA operation, we used the fundamental and DC current components derived by the conduction angle versus the input voltage magnitude as shown in Fig. 3. The RF current waveform can be defined as [10]

$$\therefore i_{ds}(\theta, v_{in}) = \begin{cases} I_q + I_{pk}(v_{in}) \cdot \cos(\theta), & -\alpha_{vin}/2 < \theta < \alpha_{vin}/2, \\ 0, & -\pi < \theta < -\alpha_{vin}/2, \alpha_{vin}/2 < \theta < \pi. \end{cases} \quad (2)$$

where I_q is the quiescent bias current and $I_{pk}(v_{in})$ is the magnitude of the drain current of the given PA. We assume that all the PAs have a constant gm versus input voltage for simplicity. The final conduction angle versus input voltage magnitude can be derived as [19]

$$\therefore \alpha_{vin} = 2 \cdot \arccos\left[\frac{V_{gsq}}{V_{gsq} - (v_{in}/V_{MAX})}\right] \cdot \frac{180}{\pi} \quad (3)$$

where, $\cos(\alpha_{vin}/2) = -\frac{I_q}{I_{pk}(v_{in})}$,

$$I_{pk}(v_{in}) = I_{in}(v_{in}) - I_q.$$

The $I_{in}(v_{in})$ is an absolute amplitude of the drain current under the given input voltage, ' v_{in} ', and it is proportional to

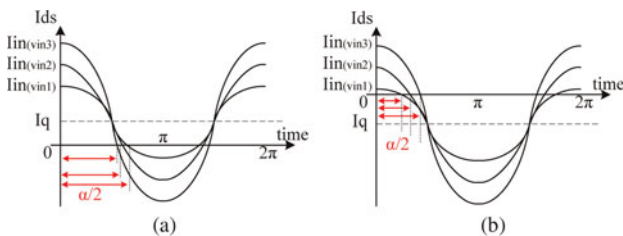


Fig. 3. The conduction angle variation versus the input power level with different bias: (a) Class AB mode and (b) Class C mode. (The I_{ds} below 0 is the cut-off level.)

the input voltage. Therefore, the fundamental and DC currents of the carrier and two peaking PAs based on each conduction angle can be defined as follows:

$$\therefore I_C(v_{in}) = \frac{I_{inC}(v_{in})}{2\pi} \cdot \frac{\alpha_{C,vin} - \sin(\alpha_{C,vin})}{1 - \cos(\alpha_{C,vin}/2)} \quad (4)$$

$$= \frac{I_{inC}(v_{in})}{2\pi} \cdot W_C,$$

$$\therefore I_{P1}(v_{in}) = \frac{I_{inP1}(v_{in})}{2\pi} \cdot \frac{\alpha_{P1,vin} - \sin(\alpha_{P1,vin})}{1 - \cos(\alpha_{P1,vin}/2)} \quad (5)$$

$$= \frac{I_{inP1}(v_{in})}{2\pi} \cdot W_{P1},$$

$$\therefore I_{P2}(v_{in}) = \frac{I_{inP2}(v_{in})}{2\pi} \cdot \frac{\alpha_{P2,vin} - \sin(\alpha_{P2,vin})}{1 - \cos(\alpha_{P2,vin}/2)} \quad (6)$$

$$= \frac{I_{inP2}(v_{in})}{2\pi} \cdot W_{P2},$$

$$\therefore I_{DC,C}(v_{in}) = \frac{I_{inC}(v_{in})}{2\pi} \cdot \frac{2 \cdot \sin(\alpha_{C,vin}/2) - \alpha_{C,vin} \cdot \cos(\alpha_{C,vin}/2)}{1 - \cos(\alpha_{C,vin}/2)} \quad (7)$$

$$= \frac{I_{inC}(v_{in})}{2\pi} \cdot Y_C$$

$$\therefore I_{DC,P1}(v_{in}) = \frac{I_{inP1}(v_{in})}{2\pi} \cdot \frac{2 \cdot \sin(\alpha_{P1,vin}/2) - \alpha_{P1,vin} \cdot \cos(\alpha_{P1,vin}/2)}{1 - \cos(\alpha_{P1,vin}/2)} \quad (8)$$

$$= \frac{I_{inP1}(v_{in})}{2\pi} \cdot Y_{P1}$$

$$\begin{aligned} \therefore I_{DC,P2}(v_{in}) &= \frac{I_{inP2}(v_{in})}{2\pi} \\ &\cdot \frac{2 \cdot \sin(\alpha_{P2,vin}/2) - \alpha_{P2,vin} \cdot \cos(\alpha_{P2,vin}/2)}{1 - \cos(\alpha_{P2,vin}/2)} \\ &= \frac{I_{inP2}(v_{in})}{2\pi} \cdot Y_{P2}, \end{aligned} \quad (9)$$

$$\alpha_{C,vin} = \begin{cases} 2 \cdot \arccos \left[\frac{V_{gsq,C}}{V_{gsq,C} - v_{in}/(k_1 \cdot V_{MAX})} \right], & 0 < \frac{v_{in}}{V_{MAX}} < k_1, \\ 2 \cdot \arccos \left(\frac{V_{gsq,C}}{V_{gsq,C} - 1} \right), & k_1 < \frac{v_{in}}{V_{MAX}} < 1, \end{cases}$$

$$\alpha_{P1,vin} = 2 \cdot \arccos \left[\frac{V_{gsq,P1}}{V_{gsq,P1} - (v_{in}/V_{MAX})} \right],$$

$$\alpha_{P2,vin} = 2 \cdot \arccos \left[\frac{V_{gsq,P2}}{V_{gsq,P2} - (v_{in}/V_{MAX})} \right],$$

$$k_1 = \frac{1 + m_1}{1 + m_1 + m_2}, \quad k_2 = \frac{1}{1 + m_1}.$$

B) Efficiency of the 3-stage Doherty PA

If all the PAs are matched to the load impedance, R_L , at the full-power state, the characteristic impedance of the output combiner can be selected as [12]

$$\begin{aligned} Z_{01} &= R_L \cdot \sqrt{\frac{m_2}{1 + m_1 + m_2}}, \\ Z_{02} &= \frac{R_L}{1 + m_1} \cdot \sqrt{m_1 \cdot m_2}, \quad Z_{03} = R_L \cdot \sqrt{m_1}. \end{aligned} \quad (10)$$

For the ease of device selection, a '1:2:2' (1: $m_1:m_2$) 3-stage Doherty PA has been investigated. Thus, k_2 and k_1 are determined to be 0.33 and 0.6, respectively, on the v_{in}/V_{MAX} axis. At the region of ' $0 \sim k_2$ ', only the carrier PA is operated, and at the region of ' $k_2 \sim k_1$ ', the carrier and peaking PA 1 are operated. All the PAs are turned on at the region of ' $k_2 \sim 1$ ' on the axis.

The ideal current source expression of the 3-stage Doherty PA at the region of ' $0 \sim 0.33$ ' is shown in Fig. 4(a). The load impedance at the carrier PA's current source can be derived as

$$\therefore R_{C,\sim k_2}(v_{in}) = \frac{Z_{01}^2 \cdot Z_{03}^2}{Z_{02}^2 \cdot R_L}. \quad (11)$$

The drain efficiency below the second back-off region can be calculated using the RF power and DC power,

$$\therefore DE_{\sim k_2}(v_{in}) = \frac{1}{4\pi \cdot R_L} \cdot \frac{I_{inC}(v_{in})}{I_{max,C}} \cdot R_{C,\sim k_2}(v_{in}) \cdot \frac{W_C^2}{Y_C}, \quad (12)$$

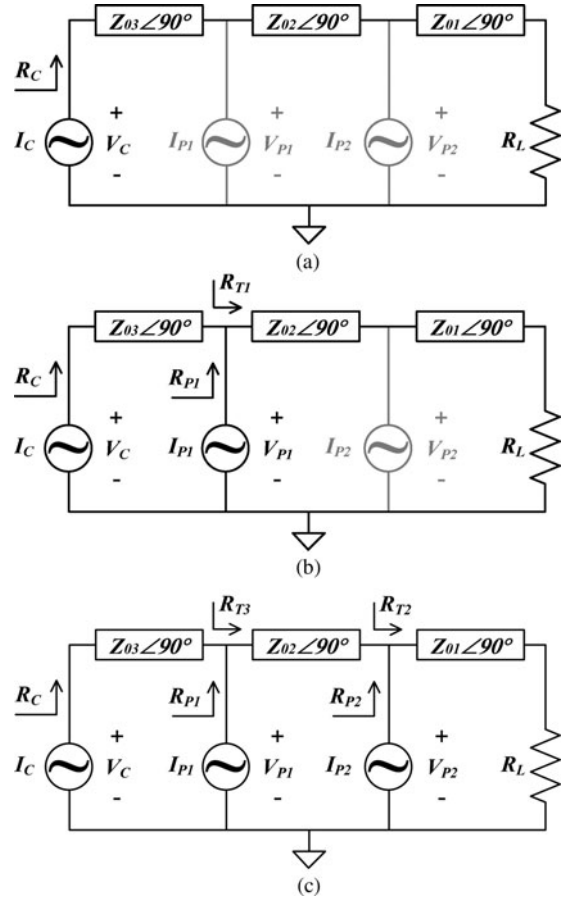


Fig. 4. The ideal current source expression of the 3-stage Doherty PA: (a) second back-off region, (b) first back-off region and (c) full-power condition. (Black: turn on state; gray: turn off state.)

where

$$P_{RF,\sim k_2}(v_{in}) = 0.5 \cdot I_C(v_{in})^2 \cdot R_{C,\sim k_2}(v_{in}),$$

$$P_{DC,\sim k_2}(v_{in}) = I_{DC,C}(v_{in}) \cdot V_{DC}.$$

Fig. 4 (b) represents the region of ' $0.33 \sim 0.6$ ', where the carrier PA and peaking PA supply the fundamental currents to the load. The fundamental drain current ratio between the carrier PA and peaking PA 1 is defined as

$$\therefore \delta_1(v_{in}) = \frac{I_{P1}(v_{in})}{I_C(v_{in})}. \quad (13)$$

The load impedance at each voltage node can be calculated using the active load-pull principle [10].

$$\therefore R_{T1}(v_{in}) = \frac{Z_{02}^2}{Z_{01}^2} \cdot R_L, \quad (14)$$

$$\therefore R_{C,\sim k_1}(v_{in}) = \frac{Z_{01}^2 \cdot Z_{03}^2}{Z_{02}^2 \cdot R_L \cdot [1 + \delta_1(v_{in})]}, \quad (15)$$

$$\therefore R_{P1,\sim k_1}(v_{in}) = \left[1 + \frac{1}{\delta_1(v_{in})} \right] \cdot \frac{Z_{02}^2}{Z_{01}^2} \cdot R_L. \quad (16)$$

The drain efficiency below the first back-off region can be calculated in the same way.

$$\begin{aligned} \therefore DE_{\sim k_1}(v_{in}) &= \frac{1}{4\pi \cdot R_L \cdot I_{max,C}} \cdot [Iin_C(v_{in})^2 \cdot W_C^2 \cdot R_{C,\sim k_1}(v_{in}) \\ &\quad + Iin_{P_1}(v_{in})^2 \cdot W_{P_1}^2 \cdot R_{P_1,\sim k_1}(v_{in})] / \\ &\quad [Iin_C(v_{in}) \cdot Y_C + m_1 \cdot Iin_{P_1}(v_{in}) \cdot Y_{P_1}], \end{aligned} \quad (17)$$

where

$$P_{RF,\sim k_1}(v_{in}) = 0.5 \cdot I_C(v_{in})^2 \cdot R_{C,\sim k_1}(v_{in}) + 0.5 \cdot I_{P_1}(v_{in})^2 \cdot R_{P_1,\sim k_1}(v_{in}),$$

$$P_{DC,\sim k_1}(v_{in}) = (I_{DC,C}(v_{in}) + I_{DC,P_1}(v_{in})) \cdot V_{DC}.$$

Fig. 4(c) represents the region of ‘0.6–1’, where all the PAs’ current sources supply the fundamental current to the load. The fundamental drain current ratio between the carrier PA and two peaking PAs is defined as

$$\therefore \delta_2(v_{in}) = \frac{I_{P_2}(v_{in})}{I_C(v_{in}) + I_{P_1}(v_{in})}. \quad (18)$$

The load impedance at each voltage node can also be calculated in the same way:

$$\therefore R_{T_2}(v_{in}) = \frac{Z_{O1}^2}{R_L}, \quad (19)$$

$$\therefore R_{P_2,\sim 1}(v_{in}) = \left[1 + \frac{1}{\delta_2(v_{in})} \right] \cdot \frac{Z_{O1}^2}{R_L}, \quad (20)$$

$$\therefore R_{T_3}(v_{in}) = \frac{Z_{O2}^2 \cdot R_L}{Z_{O1}^2 \cdot [1 + \delta_2(v_{in})]}, \quad (21)$$

$$\therefore R_{C,\sim 1}(v_{in}) = \frac{Z_{O1}^2 \cdot Z_{O3}^2}{Z_{O2}^2 \cdot R_L} \cdot \frac{1 + \delta_2(v_{in})}{1 + \delta_1(v_{in})}, \quad (22)$$

$$\therefore R_{P_1,\sim 1}(v_{in}) = \frac{Z_{O2}^2 \cdot R_L}{Z_{O1}^2} \cdot \frac{1 + \delta_1(v_{in})}{\delta_1(v_{in}) \cdot [1 + \delta_2(v_{in})]}. \quad (23)$$

The drain efficiency up to the full-power state can be calculated using the RF power and DC power,

$$\begin{aligned} \therefore DE_{\sim 1}(v_{in}) &= \frac{1}{4\pi \cdot R_L \cdot I_{max,C}} \cdot [Iin_C(v_{in})^2 \cdot W_C^2 \cdot R_{C,\sim 1}(v_{in}) \\ &\quad + Iin_{P_1}(v_{in})^2 \cdot W_{P_1}^2 \cdot R_{P_1,\sim 1}(v_{in}) \\ &\quad + Iin_{P_2}(v_{in})^2 \cdot W_{P_2}^2 \cdot R_{P_2,\sim 1}(v_{in})] / \\ &\quad [Iin_C(v_{in}) \cdot Y_C + m_1 \cdot Iin_{P_1}(v_{in}) \cdot Y_{P_1} \\ &\quad + m_2 \cdot Iin_{P_2}(v_{in}) \cdot Y_{P_2}], \end{aligned} \quad (24)$$

where

$$\begin{aligned} P_{RF,\sim 1}(v_{in}) &= 0.5 \cdot I_C(v_{in})^2 \cdot R_{C,\sim 1}(v_{in}) \\ &\quad + 0.5 \cdot I_{P_1}(v_{in})^2 \cdot R_{P_1,\sim 1}(v_{in}) \\ &\quad + 0.5 \cdot I_{P_2}(v_{in})^2 \cdot R_{P_2,\sim 1}(v_{in}), \end{aligned}$$

$$\begin{aligned} P_{DC,\sim 1}(v_{in}) &= (I_{DC,C}(v_{in}) + I_{DC,P_1}(v_{in}) \\ &\quad + I_{DC,P_2}(v_{in})) \cdot V_{DC}. \end{aligned}$$

C) Matlab simulation results of the 3-stage Doherty PA with and without adaptive gate ET operation

For simulation, the conduction angle of the carrier PA at the full-power state is set to 180° ($V_{gsq,C} = 0$), and those of the peaking PAs to 151.05° ($V_{gsq,P_1} = -0.33$) and 135.95° ($V_{gsq,P_2} = -0.6$) to turn on the PAs above the k_2 and k_1 , respectively. The 3-stage Doherty PA simulated is configured to ‘1:2:2’ unit PAs, and the drain DC bias applied is 30 V. In Fig. 5, the optimum gate bias shapes versus the normalized input voltage magnitude are illustrated, and the biases are increased from the class C mode to enhance the output power of each peaking PA as the input power level is increased. In Fig. 6, the simulation results of the 3-stage Doherty PA with and without the gate adaptation to the peaking PAs. Fig. 6(a) shows the simulated fundamental drain current increment of each PA [20]. Without the gate bias adaptation, the fundamental drain currents of the peaking PA 1 and 2 do not reach the 2 A (which is two times larger magnitude than the carrier PA’s maximum drain current) because of the low gate bias. Fig. 6(b) shows the fundamental drain voltage variation versus the normalized input voltage. As expected from Fig. 6(a), the two peaking PAs’ drain voltage do not reach 30 V. Especially, the peaking PA 2’s fundamental current and voltage show the seriously insufficient load modulation. The load impedance variation at each current source is presented in Fig. 6(c) and Table 2. All PAs do not reach the required load impedance after the ‘0.33’ of the normalized input power level. The fundamental drain current ratios, δ_1 and δ_2 , have to be increased from 0 to 2 and from 0 to 0.6, respectively. The variation of the δ_1 and δ_2 are shown in Fig. 6(d). The optimum gate biases of

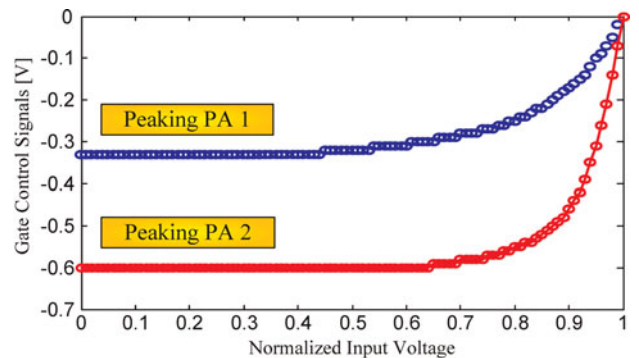


Fig. 5. The optimum gate bias shapes for the peaking PAs versus the normalized input voltage.

Table 2. The load impedance variation versus the input power level for the ‘1:2:2’ 3-stage Doherty PA with and without the gate bias adaptation

(Without/With)	0–0.33	0.33–0.6	0.6–1
Carrier	90/90 Ω	59.5/50 Ω	51.3/50 Ω
Peaking 1	∞	164.1/131.8 Ω	79.6/50 Ω
Peaking 2	∞	∞	94.5/50 Ω

each peaking PA are determined to get the proper load impedances which decide the efficiency and output power(or gain flatness) of Doherty PA versus the input voltage level. At the region of ‘0.33–0.6’ on the normalized input voltage axis, only the peaking PA 1’s gate biases is increased. As the peaking PA 1’s gate bias is increased, the fundamental drain voltage of the PA reaches the 30 V, and the load impedance is converged to ‘2.5 \cdot Ro’ of load impedance in Fig. 6(a) and (b). At the region of ‘0.6–1’, both the peaking PAs’ gate biases have to be adapted. Through the gate bias adaptation, the two peaking PAs’ fundamental drain currents reach its maximum magnitude, and the carrier PA and peaking PA 1’s fundamental drain voltages are maintained near the 30 V. The load impedances of all PAs are converged to the 50 Ω , and the proper load modulation behavior is achieved along the overall input power level. The δ_1 and δ_2 are also enhanced to 2 and 0.6, respectively.

In Fig. 7(a), the simulated load lines of each PA are illustrated, only showing the left side from V_{DC} of 30 V, for simplicity. As shown in figure, without the gate control, the minimum drain voltages of the peaking PAs do not reach the knee region. This operation causes serious degradation of efficiency for the two peaking PAs, and the overall efficiency of Doherty PA is decreased at the backed-off output power region as shown in Fig. 7(b). Therefore, the optimum gate bias has to be properly shaped such that the carrier PA and peaking PA 1’s fundamental drain voltages maintain 30 V. In this simulation, for simplicity, the two peaking PAs’ fundamental drain currents along the power level are the same with the fundamental drain current shapes of the class C mode single PAs, whose conduction angles are 151.05° and 135.95°, respectively. Without the gate control, the peaking PAs do not reach the knee region because of the improper load modulation. The improper load modulation also reduces the peak power by about 3.33 dB as shown in Fig. 7(b). Furthermore, the two peaking PAs are also of low efficiency at the backed-off output power region. The simulated gain flatness versus the output power level is depicted in Fig. 7(c). The calculated gain flatness is improved from 3.8 to 1 dB after applying the gate bias control technique, indicating more linear AM–AM response of the proposed PA.

In Fig. 8, the calculated DC and RF powers of each PA and the overall are illustrated. By applying the gate bias control technique, the RF power generation of the two

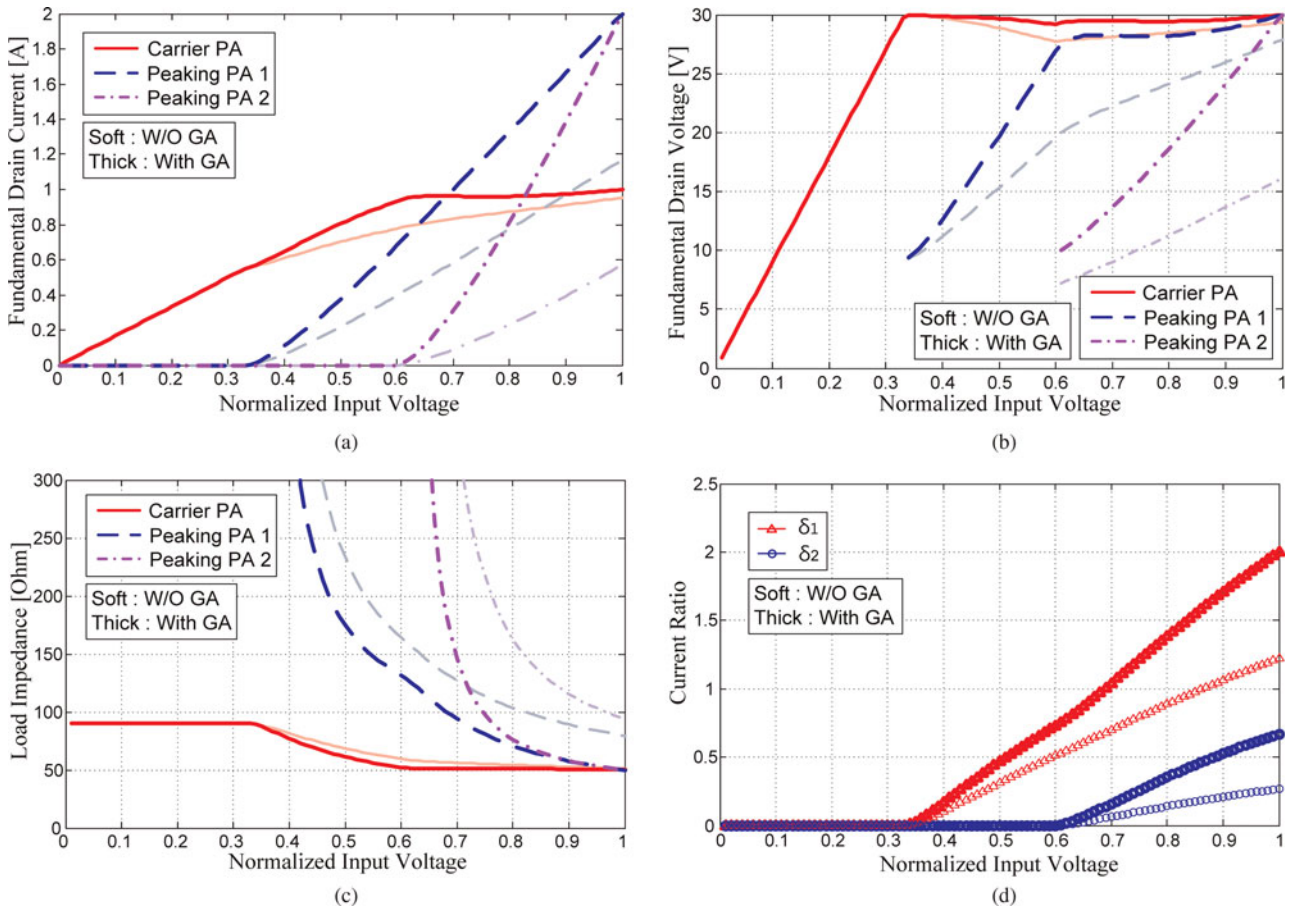


Fig. 6. The simulation result of the ‘1:2:2’ 3-stage Doherty PA with and without the gate bias adaptation(GA): (a) fundamental drain currents, (b) fundamental drain voltage, (c) fundamental load impedance at the each current source, and (d) the calculated δ_1 and δ_2 .

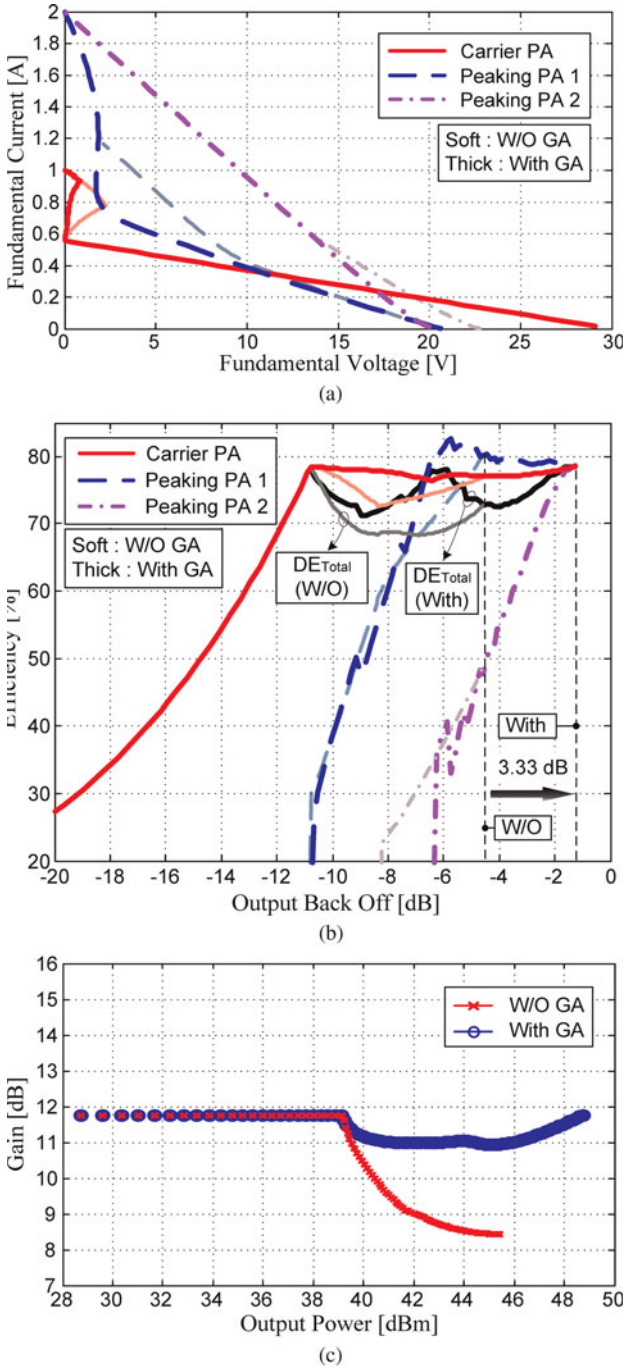


Fig. 7. The simulated (a) fundamental load-line behavior, (b) efficiency characteristic, and (c) gain characteristic of the ‘1:1.2:2’ 3-stage Doherty PA with and without the gate bias adaptation.

peaking PAs are enhanced significantly, and the 3-stage Doherty PA properly delivers the full power to the load. In Table 3, the calculated average performance of the 3-stage Doherty PA with and without the gate bias control technique are summarized for the WiMAX signal with 8.5 dB PAPR. The proposed Doherty PA shows an enhanced efficiency together with an improved average output level. These simulation results clearly show the limitation on the load modulation behavior of the conventional 3-stage Doherty PA, and the limitation can be removed by the gate bias control technique.

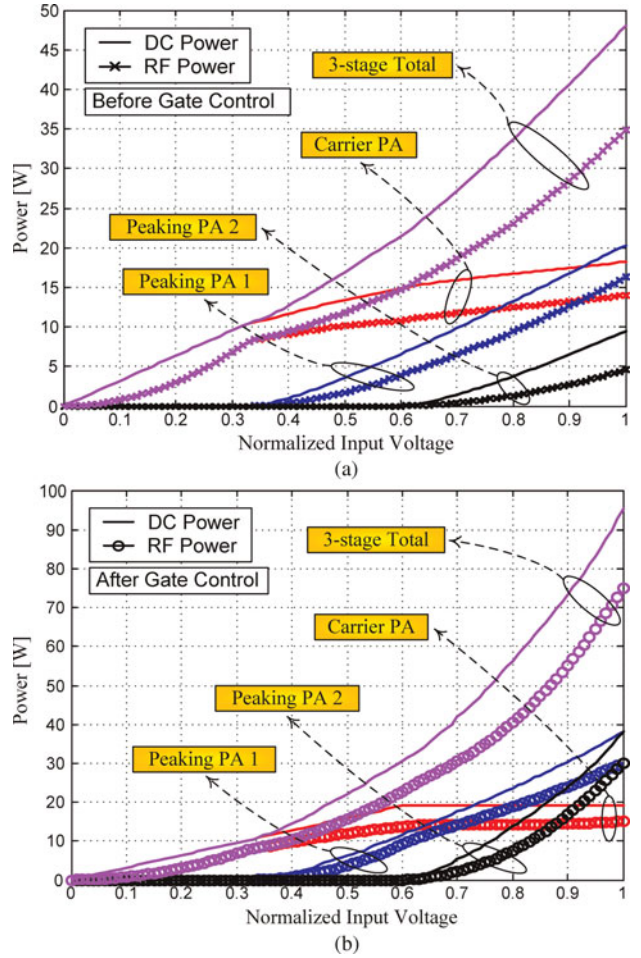


Fig. 8. The simulated DC, RF powers of each PA and total power (a) without and (b) with the gate bias adaptation.

Table 3. The calculated average performance of the 3-stage Doherty PA with and without applying the gate bias control technique for the 802.16e Mobile WiMAX signal with 8.5 dB PAPR.

Gate control	$P_{out, Avg}$	DE_{Avg}	$Gain_{Avg}$	PAE_{Avg}
Without	38.2 dBm	65.4%	10.4 dB	59.5%
With	39 dBm	68%	11.3 dB	62.9%

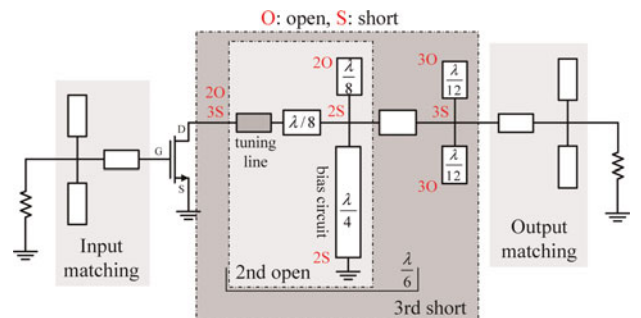


Fig. 9. The implemented circuit topology of the class F^{-1} PA.

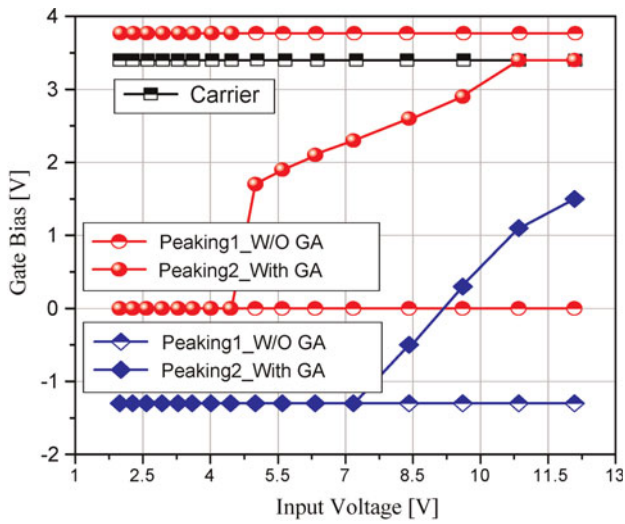


Fig. 10. The measured gate bias shapes versus input voltage.

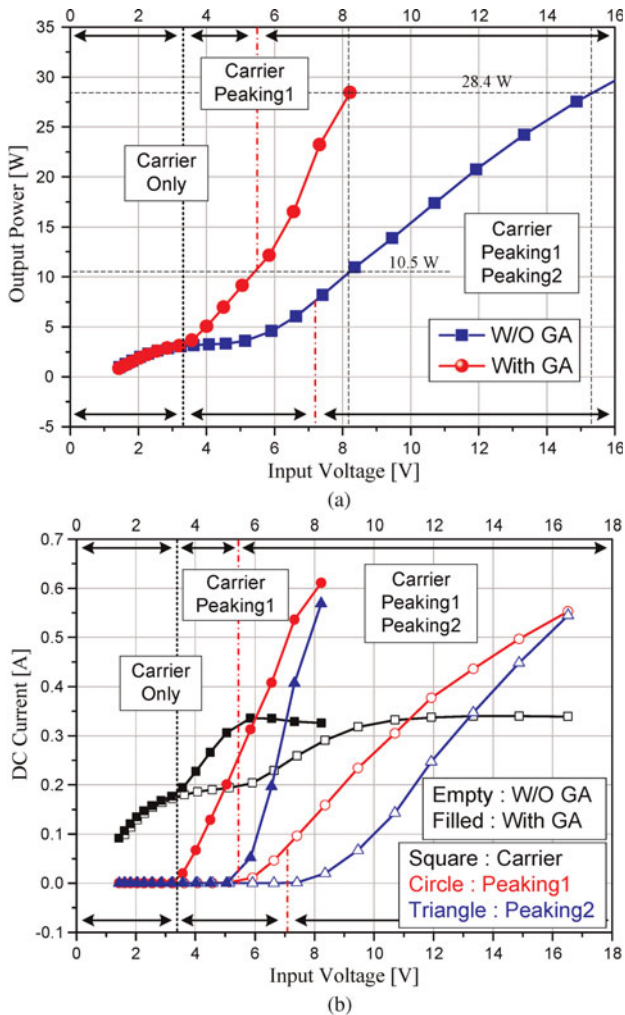


Fig. 11. The measured performances of the implemented 3-stage Doherty PA with and without the gate bias adaptation, (a) output power of the 3-stage Doherty PA and (b) DC currents of each PA versus input voltage.

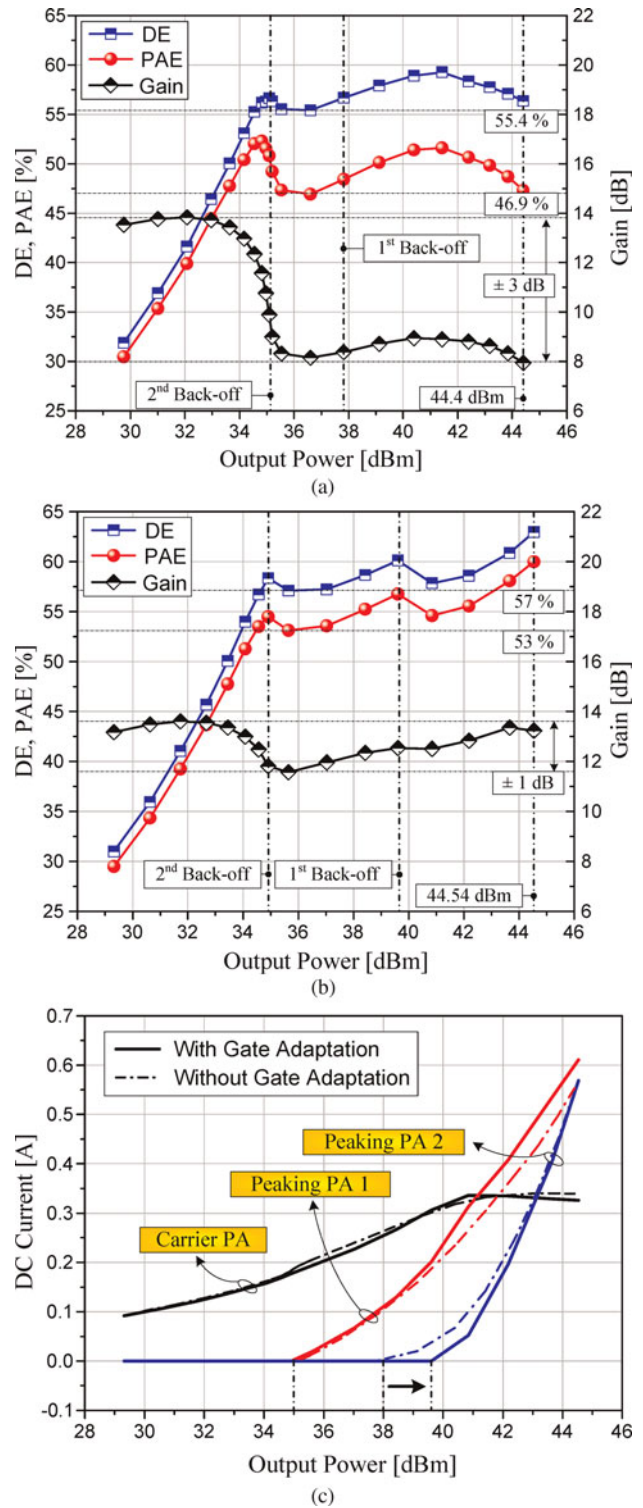


Fig. 12. The measured CW characteristics of 3-stage Doherty PA. (a) DE, PAE, and gain performance without and (b) with the gate bias control, and (c) DC current characteristics.

IV. IMPLEMENTATION AND MEASURED RESULTS

A) Class F^{-1} PA for the unit cell

To maximize the efficiency of the proposed 3-stage Doherty PA, we have employed a class F^{-1} PA as an unit cell shown

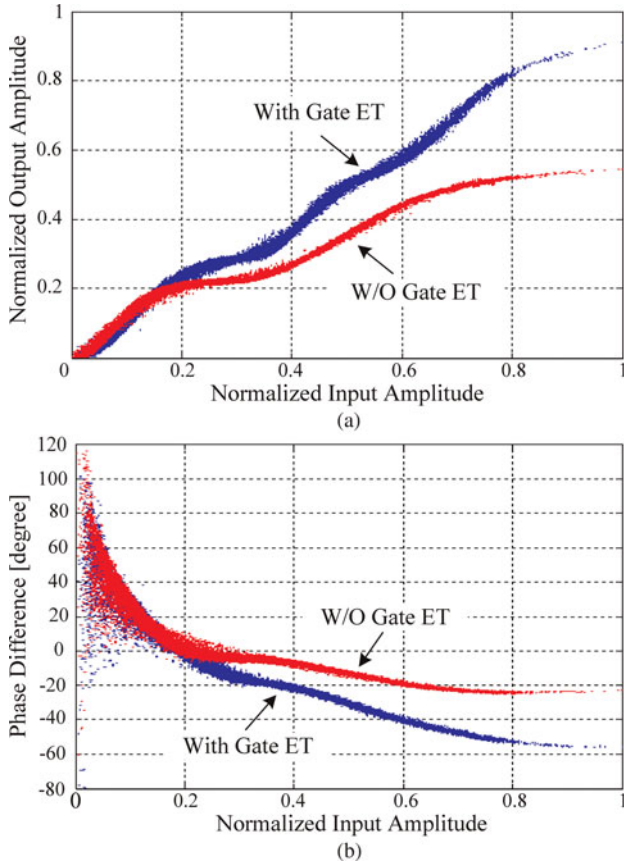


Fig. 13. Measured AM-AM and AM-PM characteristics of the 3-stage Doherty PA with and without the ET technique: (a) AM-AM, and (b) AM-PM.

in Fig. 9 [21]. The harmonic control circuit provides an open impedance at the second harmonic and a short impedance at the third harmonic. The harmonic control impedances are provided at the drain current node inside of the intrinsic capacitive components and the packing elements. Accordingly, the control circuit includes both-arm shunt stubs for better harmonic trap and tuning lines to compensate the de-tuning effects of the device's parasitic passive components [22]. The output matching network has been designed considering the impedance mismatch by the non-linear capacitive components. We have implemented the PAs using 5 W PEP MRF281S and 10 W PEP MRF282S

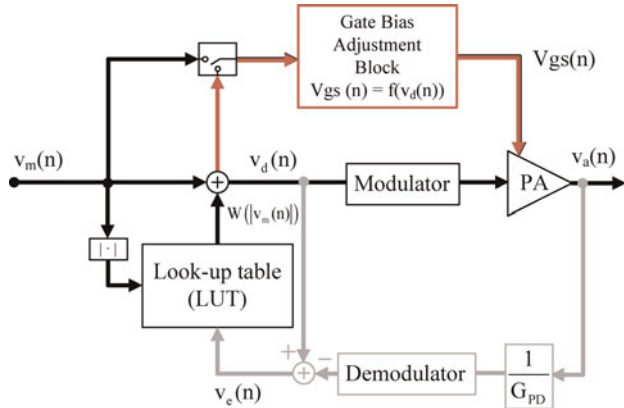


Fig. 14. The DFBPD algorithm for the ET 3-stage Doherty PA.

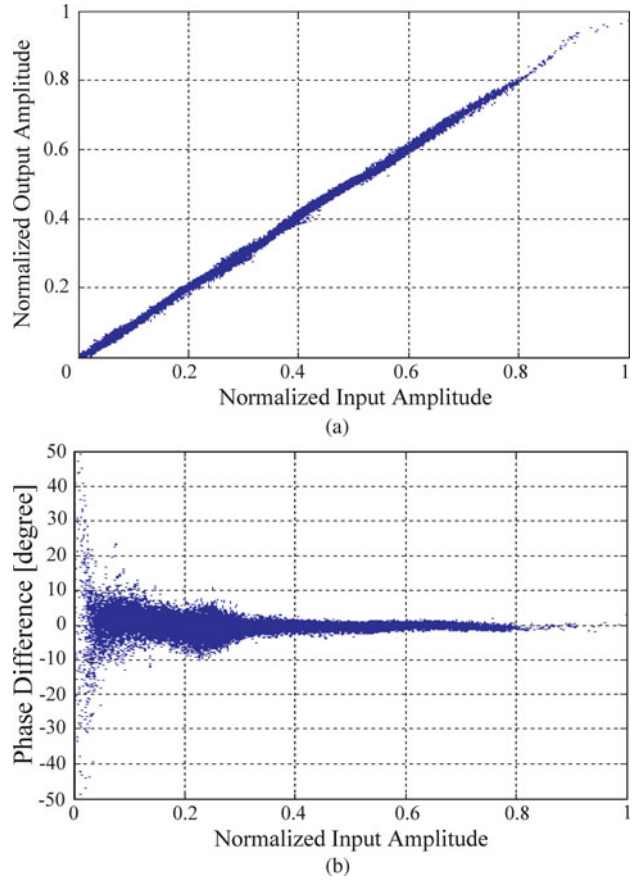


Fig. 15. Measured AM-AM and AM-PM characteristics of the 3-stage Doherty PA after linearization: (a) AM-AM, and (b) AM-PM.

LDMOSFETs and the quiescent gate bias voltages of each PA are 3.2 and 3.4 V, a class B mode, respectively, under the 30 V of a drain bias at 1 GHz. The unit PA for the carrier PA has a 71.3% of drain efficiency at an output power of 38.7 dBm, and the PA for the peaking PA has been obtained as 71.4% of drain efficiency at an output power of 41.6 dBm. The PA's output impedance for the

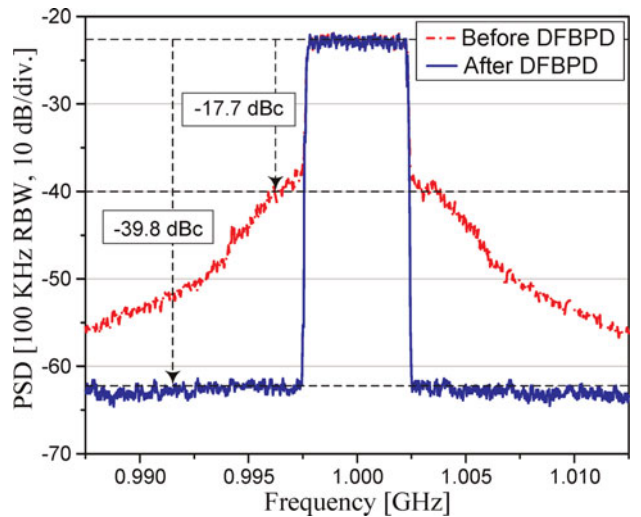


Fig. 16. Measured output spectrum of the ET 3-stage Doherty PA before and after the linearization at an average output power of 37 dBm.

Table 4. The measured average performances of the 3-stage Doherty PA with and without the gate bias control for the 802.16e Mobile WiMAX signal with 8.5 dB PAPR.

	W/O ET	With ET	With ET [DFBPD]
$P_{out, Avg}$	37 dBm	37 dBm	36.85 dBm
DE_{Avg}	56.82%	56.82%	55.46%
$Gain_{Avg}$	9.65 dB	12.15 dB	12.23 dB
PAE_{Avg}	50.66%	53.36%	52.14%
RCE	-17.12 dB	-16.22 dB	-37.23 dB

peaking PA is measured to be 652Ω after the offset line (phase offset = 92.9°).

B) Measured results for the CW signal

Fig. 10 shows the measured optimum gate bias control shapes versus the input power level. A constant gate bias is applied to the carrier PA. The gate biases of the other PAs are maintained at a deep class C mode initially for the completely turned-off operation. Above each backed-off average output power, each PA's gate biases are increased to the class B mode to accelerate the load modulation. To investigate the load modulation behavior with and without applying the gate bias control technique, the output power of the 3-stage Doherty PA and the DC current profiles of each PA versus the input voltage are measured and depicted in Fig. 11. When the proposed Doherty PA reaches the peak power of 28.4 W, the Doherty PA without the gate bias adaptation generates a 10.5 W of output power. To achieve the same peak power from the latter Doherty PA, an almost two times larger input voltage is required than that of the proposed Doherty PA. Fig. 11(b) clearly shows that the peak power degradation of the latter Doherty PA is caused by the insufficient input drive to the peaking PA. Because of the insufficient drive, the δ_1 and δ_2 are reduced, and the carrier PA's load impedance cannot be fully modulated, decreasing the carrier PA's output power as shown in Fig. 8 earlier. To generate the full peak power from the 3-stage Doherty PA without gate bias control technique, a large input power has to be applied. In this case, the carrier PA is driven into a hard saturation state, which causes a problem for the stability or reliability. In the experiment with a 1-tone signal, we have measured the performances of the two PAs for the DE, gain, and power-added efficiency (PAE) characteristics and compared them. The measured results versus the output power

level are summarized in Fig. 12. The large difference between the two PAs is a serious gain degradation because of the improper load modulation, and it causes a serious PAE degradation. Above the second backed-off output power region, the 3-stage Doherty PA without gate control has a 46.9% of PAE and a ± 3 dB of gain flatness. On the other hand, the proposed PA has a considerably improved PAE and gain flatness, 53% and ± 1 dB, respectively. To achieve the same peak power from the 3-stage Doherty PA without gate bias control, a 5.3 dB more input power is needed. Because of the gate break-down problem, the gate bias cannot be lowered enough to turn off the peaking PA when high input power is applied. As shown in Fig. 12(c), the peaking PA 2 without the gate control case is turned on early before the proper backed-off output power level in spite of the -2.6 V of low gate bias, reducing the efficiency at the backed-off output power region. With the gate bias adaptation, the peaking PAs are accurately turned on at the desirable output power, and the efficiency above the second backed-off output power region reaches the desired value.

C) Measured results for the modulation signal and linearization

Using the gate bias shaping functions shown in Fig. 10, the ET signals for each peaking PA are generated by the Matlab simulator. The generated signals are downloaded to Agilent's ESG4438C signal source and applied to the peaking PA's gate bias network through the gate driver circuit, which consists of the TI's THS3001 OP-Amp.

The measured AM-AM and AM-PM responses of the 3-stage Doherty PA with and without the ET technique are shown in Fig. 13. Owing to the large gain degradation of the 3-stage Doherty PA without the ET technique, it has a highly saturated curve on the AM-AM response. On the other hand, the proposed PA's AM-AM response is considerably linearized. However, the proposed PA as a even worse amplitude modulation-phase modulation (AM-PM) response because the gate bias control is not optimized for linearity, but the load modulation behavior for the flat gain response and peak power. To linearize the proposed PA, the digital feedback predistortion (DFBPD) has been applied to the RF input signal and the gate bias [1], as shown in Fig. 14. The linearized AM-AM and AM-PM responses of the proposed 3-stage Doherty PA are shown in Fig. 15, and the output spectra before and after the linearization for the WiMAX

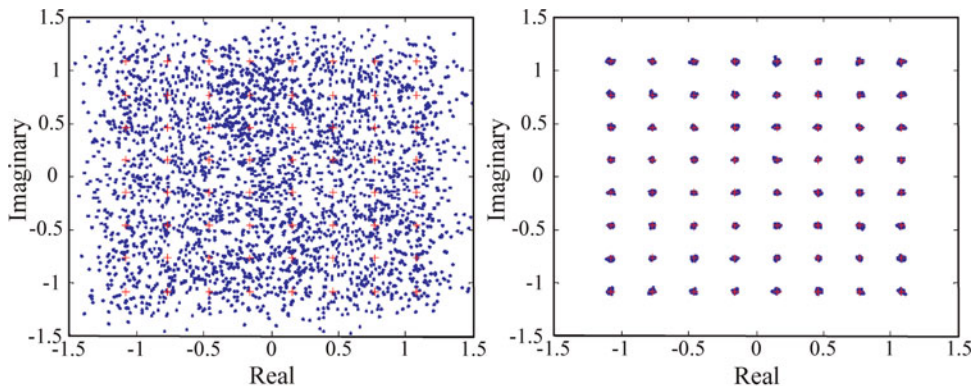


Fig. 17. Measured signal constellation diagrams of the ET 3-stage Doherty PA, before (left) and after (right) linearization.

signal with the 8.5 dB PAPR are presented in Fig. 16. By employing the DFBPD algorithm, the adjacent channel leakage ratio (ACLR) at the 3.572-MHz offset is linearized to -39.8 dBc, and the performance is summarized in Table 4. Comparing the PAs with and without the ET, the PAE characteristic of the proposed 3-stage Doherty PA is improved by about 2.7% with the 2.5 dB-enhanced gain at the same average output power of 37 dBm. After linearization, the proposed PA has 52.14% and 55.46% of high PAE and DE, respectively, at an average output power of 36.85 dBm which is a 7.7 dB backed-off output power level from the peak power. The relative constellation error (RCE) is also enhanced to -37.23 dB, successfully satisfying the system specification. The constellation diagrams before and after the linearization of the proposed 3-stage Doherty PA are shown in Fig. 17. These experimental results clearly show that the proposed 3-stage Doherty PA with the ET technique has a high efficiency with high peak power, and it is suitable for a linear transmitter.

V. CONCLUSIONS

We have suggested an optimized 3-stage Doherty PA with the ET technique to achieve the high peak power and maximum efficiency at the backed-off output power region. It is verified through Matlab simulation for the operational behavior of the PA that the 3-stage Doherty PA has the best flat efficiency versus the output power level among the various Doherty architecture. However, we have found that the PA has a seriously improper load modulation, and the proper load modulation behavior can be achieved by applying the gate bias control technique. For verification, 5 W and 10 W PEP LD MOSFETs have been used for the unit PA at 1-GHz, which is a class F^{-1} to maximize the efficiency of the PA. In the experiment, the gate bias adaptation is optimized for the accurate and maximally efficient Doherty operation. The proposed 3-stage Doherty PA has improved the gain and PAE by 2.5 dB and 2.7%, respectively, at the same average output power of 37 dBm by employing the ET technique. After the linearization, the proposed PA shows 52.14% and 55.46% of PAE and DE characteristics, respectively, at an average output power of 36.85 dBm, a 7.7 dB backed-off output power level. The RCE is -37.23 dB, satisfying the system specification. Therefore, it is clearly verified that the ET 3-stage Doherty PA using the saturated PA is a very powerful architecture for high efficiency, and the proposed gate bias control method employing ET technique is essential for the proper load modulation behavior. This architecture is suitable for the highly efficient and linear transmitter.

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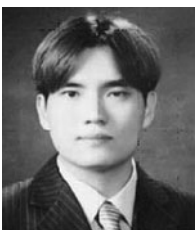
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